Abstract

It is a widely supported prediction that conventional computer hardware technologies are going to reach their limits in the near future. Consequently, researchers are working on alternatives. Reversible circuits and quantum circuits are one promising direction which allows to overcome fundamental barriers. However, no real design flow for this new kind of circuits exists so far. Physical implementations are in its infancy. Within this seminar, recent research questions of this emerging technology have been discussed.


1998 ACM Subject Classification B.6 Logic Design, D.1 Programming Techniques, F.2 Analysis of Algorithms and Problem Complexity, I. Computing Methodologies

Keywords and phrases reversible computation, quantum computation, computer aided design, hardware and software design, physical implementation, applications


1 Executive Summary

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The development of computing machines found great success in the last decades. But the ongoing miniaturization of integrated circuits will reach its limits in the near future. Shrinking transistor sizes and power dissipation are the major barriers in the development of smaller and more powerful circuits. To further satisfy the needs for more computational power and further miniaturization, alternatives are needed that go beyond the scope of conventional technologies like CMOS. Reversible logic and quantum logic provide a promising alternative that may enhance or even replace conventional circuits in the future. More precisely:

- **Low Power Computation**
  While conventional circuits dissipate energy for each lost bit of information, reversible circuits are information lossless, i.e. theoretically they are not affected by this. Considering the increasing miniaturization, this makes reversible logic interesting for domains like low-power design. Besides this general paradigm, reversible circuits are particularly suited for complementary low-power solutions like adiabatic circuits or on-chip interconnect encoders.

- **Quantum Computation**
  Quantum Computation offers the promise of more efficient computing for problems that are of exponential difficulty for conventional computing paradigms. Considering that many of the established quantum algorithms include a significant Boolean component...
(e.g. the oracle transformation in the Deutsch-Jozsa algorithm, the database in Grover's search algorithm, and the modulo exponentiation in Shor's algorithm), it is crucial to have efficient methods to synthesize quantum gate realisations of Boolean functions. Since any quantum operation inherently is reversible, reversible circuits can be exploited for this purpose.

However, no real design flow for these new kinds of circuits exists so far. Proposed approaches for synthesis, verification, and test are only applicable for very small circuits and systems. This is crucial since the design for reversible and quantum systems significantly differs from their conventional counterparts. Nearly all concepts and methods developed for conventional hardware design in the last decades have to be redeveloped in order to support the new technologies. Additionally, considering that today researchers are still faced with serious challenges for conventional technologies, it is worth working towards design solutions for reversible and quantum technologies already today.

The goal of the seminar was to bring together experts in order to present and to develop new ideas and concepts for the design of complex reversible and quantum circuits. In total, 17 presentations together with 1 tool demonstration (of the open source toolkit RevKit) and one panel sessions (on the different opinions on how reversible circuits can help to reduce power consumption during computation) have been conducted within the seminar. This has been accompanied by several working group and proposal preparation meetings. The most important topics which have been discussed were:

- **Design Methods**
  *How to (automatically) synthesize reversible and quantum circuits as well as check them for correctness?*
  Most of today's synthesis approaches for reversible and quantum circuits still rely on Boolean function descriptions like e.g. permutations, truth tables, or binary decision diagrams. In order to design complex circuits, higher levels of abstractions have to be considered. While for this purpose hardware description languages like VHDL, SystemC, or SystemVerilog have been established in conventional hardware design, high level synthesis of reversible and quantum circuits is just at the beginning. In order to advance this area, ideas about concepts, languages, and synthesis approaches for high level design have been presented and collected at the seminar.

- **Theoretical Consideration**
  *How can theoretical studies show us the way for realizing reversible/quantum computers?*
  In order to implement efficient reversible/quantum circuits and computers, we still need very basic and theoretical studies on them. This is because the paradigm of reversible/quantum computing has very different natures from that of conventional computing. Therefore, we shall still be able to find many novel and useful ideas for them through theoretical studies. In this seminar, theoretical consideration on various models in several levels have been presented and discussed. These models range from the element level to the software level, which include reversible logic elements and circuits, quantum automata, reversible Turing machines, and reversible programming languages.

- **Physical Realizations and Accuracy of Models**
  *How to physically implement the respective circuits?*
  *How to close the gap between the theoretical models and the physical implementation?*
  In order to design reversible and quantum circuits, abstractions of the precise physical realizations are applied. These include the used gate library and the respective cost metrics, but also fault models for testing or abstractions for technology mapping. Due
to the progress in the development of physical realizations, these models constantly are subject to modifications which needed to be considered in the design phase. During the seminar, recent achievements in the development of physical realizations have been presented. This built the basis for discussions about updating and refining the applied models and abstractions.

Applications

How can reversible and quantum circuits be exploited in practically relevant application? How to measure and proof the benefits of these emerging technologies (e.g. how to substantiate improvements in the power consumption)?

So far, design methods have mostly been applied to “academic” examples only. However, the design of reversible circuits for precise applications is the next logical step. Possible directions (e.g. in the low-power domain) have been discussed at the seminar. This also included discussions of the requirements for such applications and how the benefits can be measured.

Results of the seminar are currently used in the preparation of upcoming scientific papers. As one example, a special issue on the results triggered by the ideas of this seminar is planned for 2013. Furthermore, the discussions encouraged the preparation of proposals for national and international research projects.
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3 Overview of Talks

3.1 What do reversible Turing machines compute?

Holger Bock Axelsen (University of Copenhagen, DK)

We gave an overview of recent computability and complexity results for reversible Turing machines. We showed that garbage-free reversible Turing machines (without an extraneous input copy in its output) can compute injective functions only, but that all injective, computable functions are in range [1]. We gave a definition of universality for reversible programs, and briefly outlined a universal reversible Turing machine [2]. Moving on to computational complexity, we discussed some consequences of tape reduction [3], and raised the question of whether analogous results are obtainable for reversible circuits.

References

3.2 Reversible CMOS computers

Alexis De Vos (Gent University, BE)

CMOS (complementary metal-oxide-semiconductor) technology is the standard silicon technology for fabricating every-day electronic chips.

Applying the same transistor technology, but replacing AND, NAND, OR, NOR, and XOR gates by reversible gates, such as NOT gates, Feynman gates, Toffoli gates, and Fredkin gates, allows to build (classical) reversible circuits, i.e. chips that can compute either forwards or backwards, according to the applied driving force (i.e. applied voltages).

By using so-called adiabatic input signals (i.e. smooth voltage ramps), combined with dual-logic pass-transistor architecture, in principle, energy consumption per elementary computational step can be made arbitrarily small, and thus smaller than the Landauer limit. However, there is a fundamental trade-off with speed: the Landauer barrier can only be crossed if computing happens sufficiently slowly. A more practical obstacle is the threshold voltage of standard transistors. Only zero-threshold transistors can guarantee asymptotically zero energy consumption.

Standard threshold voltages lead to a more modest result: a reduction of the energy consumption by about a factor 10, compared to conventional digital circuit design.

References
3.3 Reversible Logic Synthesis via Template Matching

Gerhard W. Dueck (University of New Brunswick at Fredericton, CA)

A review of reversible logic synthesis is presented. Heuristic synthesis of reversible circuits can be divided in two parts. First, find a reversible circuit (the circuit may be far from optimal). Second, optimize the circuit. One way to optimize the circuit is by applying rewriting rules, also known as templates. In this talk we prove two new results regarding template matching. First, the traditional definition of template does not guarantee minimality, since some templates are discarded. Secondly, we conjecture that given all templates with m lines and an exact template matching method an optimal circuit can be found for any circuit with m lines. A new solution for exact template matching is discussed. It should be feasible to find all templates with three lines. It remains to be seen how much reduction is possible for circuits with more than three lines. Some directions for further work are given.

3.4 Quantum Finite automata on infinite words

Rusins Martins Freivalds (University of Latvia, LV)

The definition of language recognition by quantum finite automata in the case when the language consists of infinite words is somewhat non-trivial because there is no easy way how to consider a measurement after processing an infinite word. However a natural definition is possible based on measure theory developed by E.Borel and the standard definition of language recognition by deterministic and nondeterministic finite automata in the case when the language consists of infinite words developed by R.Büchi. We prove that Measure-Many finite quantum automata can recognize with probability 1 languages not recognizable by deterministic and nondeterministic finite automata. On the other hand, Measure-Once finite quantum automata can recognize with a bounded error only languages recognizable by deterministic finite automata.

3.5 Formal Verification of Quantum Systems

Simon Gay (University of Glasgow, GB)

The field of formal methods is well established in classical computing. It defines formal languages in which to model systems and specify their desired properties, theories in which to express satisfaction of specifications by systems, and automated tools for verification. A range of formal methods techniques and tools have been applied to the analysis of classical
computing systems, especially concurrent and distributed systems, in diverse areas including networking, security, and safety-critical systems.

During the last several years, my collaborators and I have been developing formal methods for quantum systems and, more generally, systems that combine classical and quantum computation and communication. Our results include development of the theory of quantum process calculus, and a prototype model-checking tool for automatic verification of quantum systems (for example, communication protocols).

In my talk I motivated this research programme, argued that formal specification and verification should form part of the design process and tool chain for quantum systems, and presented a selection of results. The talk included a demonstration of the quantum model-checking tool QMC.

3.6 Principles of Reversible Computing

Robert Glück (University of Copenhagen, DK)

We presented the main principles of reversible programming languages and discussed their relation to the design of reversible computer hardware. This includes a clear distinction between the mathematical specification and the operational properties of reversible programs which manifests itself in two main design steps: injectivization of the functional specification and the reversibilization of a program. The simple reversible programming language Janus was introduced as well as design principles for "good" reversible programming languages. We also outlined the main direction for what one may call 'reversible computing science'.

References

3.7 Quantum Automata Theory – A Review

*Mika Hirvensalo (University of Turku, FI)*

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URL http://dx.doi.org/10.4018/jncr.2010010104

The main models of quantum finite automata are presented and their main properties are reviewed.

Measure-once -model by Moore and Crutchfield [5] is presented as a natural variant of probabilistic automata [6]. A further variant, Measure-many automata [4] were introduced by Kondacs and Watrous to enhance the language recognition capability. Ambainis & al. introduced Latvian automata [1], a model with more elegant closure properties and algebraic characterization. Hirvensalo [2], [3] introduced quantum automata with open time evolution, and this model can be seen as a true generalization, not only variant, of classical finite automata.

References


3.8 Describing and Optimizing Reversible Logic using a Functional Language

*Michael Kirkedal Thomsen (University of Copenhagen, DK)*

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The presentation showed the design of a language for the description and optimization of reversible logic circuits. The language is functional and based on combinators, where the most recognizable of these combinators is inversion, $\beta f$, that defines the inverse function of $f$ using an efficient semantics.

It is important to ensure that all language constructs are reversible and for this language we will, furthermore, require that this is done by static analysis only.

For most reversible languages a run-time analysis is needed, but for circuit design a run-time check of the description is undesirable.
Future work will show that the combination of the functional language and the restricted reversible model will allow more possibilities in the term rewriting and, thus, we expect to do a better optimization that other optimization techniques for reversible circuits.

References
3.9 Decision Diagram Techniques for Reversible and Quantum Circuit Equivalence Checking

D. Michael Miller (University of Victoria, CA)

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Joint work of Miller, D. Michael; Wille, Robert; Grosse, Daniel; Drechsler, Rolf


URL http://dx.doi.org/10.1109/ISMVL.2009.19

The first part of this presentation is tutorial in nature. It reviews a selection of decision diagram techniques and how they have been applied to matrix representation for reversible and quantum circuits. The second part of the presentation shows how decision diagrams can be used to check the equivalence of two circuits regardless of the number of ancillary inputs and garbage outputs using novel techniques employing simple matrix operations.

The presentation addresses reversible circuits with binary inputs and outputs, but it is readily extended to the multiple-valued case, and to general quantum circuits. While this method has been developed using one particular type of decision diagram, QMDD, it should be straightforward to implement it using other decision diagram structures developed for quantum gates and circuits.

3.10 Permutation Decision Diagrams (πDDs) and Analysis of Primitive Sorting Networks

Shin-ichi Minato (Hokkaido University, JP)

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URL http://dx.doi.org/10.1007/978-3-642-21581-0_9

Recently, we proposed a new type of decision diagram named “πDD,” for compact and canonical representation of a set of permutations. Similarly to an ordinary BDD or ZDD, πDD has efficient algebraic set operations such as union, intersection, etc. In addition, πDDs have a special Cartesian product operation which generates all possible composite permutations for two given sets of permutations. This is a beautiful and powerful property of πDDs.

In this talk, we present “permutation family algebra” based on πDDs, and how to describe and solve permutational problems using the algebra. We also show an application of πDDs for analyzing primitive sorting networks.

We succeeded in calculating the number of ways to construct minimum primitive sorting networks as 2,752,596,959,306,389,652 for $n = 13$, which has not been known in the past, where $n$ is the width of the primitive sorting network.
3.11 Reversible logic elements with memory

Kenichi Morita (Hiroshima University, JP)

We investigate a possibility of using reversible logic elements with memory (RLEM) as primitives for constructing reversible computing systems, from a theoretical standpoint. One of the characteristics of RLEMs is that there is no need to synchronize two or more input signals as in the case of reversible logic gates, because, in an RLEM, an incoming signal interacts only with its internal state, a stationary information. Another feature of an RLEM is that it can be modeled by an idealized physically reversible mechanical system easily, though its practical implementation in a reversible physical system is still very difficult as in the case of reversible gates. An important property of RLEMs is that some models of computing systems such as reversible Turing machines can be constructed by using a suitable RLEM very simply. We also discuss universality/non-universality of RLEMs. In the case of 2-state RLEMs, all but only four among the infinite kinds of RLEMs are universal in the sense that any reversible Turing machine can be built by each of them.

3.12 Realization of Reversible Gates with New Quantum Gate Libraries

Zahra Sasanian (University of Victoria, CA)

The synthesized reversible circuits are usually evaluated based on quantum cost models. The most common quantum library for realizing a class of reversible gates called Multiple-Control Toffoli (MCT) gates is the NCV (NOT, CNOT, V, and V+) library. We presented two new quantum gate libraries as the target for technology mapping MCT cascades and showed their advantages over the well-known NCV library. The first new quantum library, NCVW, contains all the gates in the NCV library plus a gate implementing a fourth root of the NOT gate called the W gate and its inverse gate denoted by W+. The second new library includes NCV gates that are controlled by the quantum value, V1, instead of zero or one. A linear decomposition structure has also been proposed that utilizes this library to realize MCT gates with low linear quantum cost. The experimental results show that using these target libraries lead to less expensive circuits in terms of the number of gates compared to NCV circuits.

Mathias Soeken (Universität Bremen, DE)

RevKit is an open source toolkit for reversible circuit design. The motivation behind it is to make recent developments in the domain of reversible circuit design accessible to other researchers. Many approaches which are only available either independently or not at all can now be used under a common hood. This allows for the integration of different techniques in order to create new work flows. Furthermore, a C++ API and a Python interface make it possible to integrate own approaches. In this sense, RevKit addresses users who simply want to apply the framework and its tools as well as developers who actively want to develop further methods on top of the framework. RevKit is available at www.revkit.org.

References


3.14 Testing and fault tolerance of reversible logic

Mehdi B. Tahoori (KIT – Karlsruhe Institute of Technology, DE)

Due to anticipated high failure rate of the emerging technologies to be used for realization of reversible logic, thorough testing and fault tolerance are crucial aspects in reversible circuits. Fault masking techniques (to prevent error propagation) for reversible logic are presented and different implementations of reversible majority voters are shown. Using voter insertion techniques and taking advantage of available non-functional outputs, we are able to provide diagnosis information with adjustable resolution for reversible circuits. Such diagnosability has important applications in manufacturing testing as well as online repair. In contrast to previous work this voter is robust against single point of failure. We target missing and repeated gate fault models which are specific to reversible logic [1].

Also, an approach for online detection of faults in reversible circuits is presented. In this approach, reversible gates are modified in such a way that they can produce information on the number of cascaded gates. By using such information an appropriate reversible gate is added to detect missing and repeated gate faults [2].

By taking advantage of reversibility of these circuits, a new testing approach for reversible circuits is developed. In this method, the next test pattern is the response of the reversible circuit to the previous test pattern. This approach requires small amount of test information which makes it suitable for BIST implementation [3].
3.15 Challenges in the Synthesis of Reversible Circuits: Today and Tomorrow

Robert Wille (Universität Bremen, DE)

In the last decade, significant progress in the development of design methods for reversible circuits has been made. First synthesis approaches relied on function representations like truth tables or permutations. They enabled synthesis of reversible circuits with a minimal number of circuit lines, but were applicable to quite small functions only. As a result, researchers strived for more scalable synthesis approaches leading e.g. to ESOP-based synthesis, BDD-based synthesis or synthesis based on the preliminary hardware description language SyReC. While they enabled synthesis of more complex functions, they usually lead to circuits with too many circuit lines. Hence, after solving the “scalability”-problem, how to keep the number of circuit lines small remains as important research question.

References

3.16 Logic level circuit optimization for topological quantum computation

Shigeru Yamashita (Ritsumeikan University – Shiga, JP)

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Joint work of Yamashita, Shigeru; Devitt, Simon; Nemoto, Kae;

I formulated the logic level circuit optimization problem for topological quantum computation. Observing the properties of "braiding operations" in topological quantum computation, I formulated our problem as to find a good gate order and a good initial qubit order.

I then presented some heuristics for the problem.

3.17 A High-Level Reversible Programming Language

Tetsuo Yokoyama (Nanzan University, JP)

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We presented a summarizing talk that covered previous work on programming methodology in reversible computing including developing a better language for writing reversible programming, better ways to write reversible programming, and the fundamental concepts on reversible languages. First, we attempted to share brief overview of a high-level reversible programming language Janus.

Next, apart from particular computational models, the fundamental problems of irreversibility and approaches to their solutions were identified. The source of irreversibility stems from irreversible data update and backward nondeterministic control flow. The solutions for avoiding those irreversibility are mainly divided into unclean and clean approaches. The superiority of clean approach was discussed by using Janus, which is a clean reversible language.

Then, we described the details on programming techniques in a high-level reversible programming language. As other programming paradigms do, reversible programming gives us opportunity to access to its own way of modularity. After that, properties of reversible programming languages were briefly discussed. We posed a few of our current research questions. Our recent result on the domain-specific optimization of reversible simulation, twice as fast as Bennett method, is represented in the form of reversible logic gates, to show the potential usefulness of the reversible simulation in the domain-specific optimization of reversible logic gates.
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