Runtime Instrumentation for Reactive Components

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Abstract

Reactive software calls for instrumentation methods that uphold the reactive attributes of systems. Runtime verification imposes another demand on the instrumentation, namely that the trace event sequences it reports to monitors are *sound* – that is, they reflect actual executions of the system under scrutiny. This paper presents RIARC, a novel decentralised instrumentation algorithm for outline monitors meeting these two demands. Asynchrony in reactive software complicates the instrumentation due to potential trace event loss or reordering. RIARC overcomes these challenges using a next-hop IP routing approach to rearrange and report events soundly to monitors.

RIARC is validated in two ways. We subject its corresponding implementation to rigorous systematic testing to confirm its correctness. In addition, we assess this implementation via extensive empirical experiments, subjecting it to large realistic workloads to ascertain its reactiveness. Our results show that RIARC optimises its memory and scheduler usage to maintain latency feasible for soft real-time applications. We also compare RIARC to inline and centralised monitoring, revealing that it induces comparable latency to inline monitoring in moderate concurrency settings where software performs long-running, computationally-intensive tasks, such as in Big Data stream processing.

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1 Introduction

Modern software is generally built in terms of concurrent components that execute without relying on a global clock or shared state [87]. Instead, components interact via non-blocking messaging, creating a loosely-coupled architecture known as a *reactive system* [9, 94], which

- responds in a timely manner (is *responsive*),
- remains available in the face of failure (is *resilient*),

- reacts to inputs from users or their environment (is *message-driven*), and
- grows and shrinks to accommodate varying computational loads (is *elastic*).

The real-world behaviour of reactive systems is hard to understand statically, and *monitoring* is used to inspect their operation at *runtime*, e.g. for debugging [111], security checking [62], profiling [76], resource usage analysis [36], etc. This paper considers runtime verification (RV), an application of monitoring used to detect whether the *current* execution of a system under scrutiny (SuS) deviates from its correct behaviour [17, 71, 22]. A RV monitor is a *sequence recogniser* [123, 101]: a state machine that incrementally analyses a *finite* fragment of the runtime information exhibited by a SuS to reach an *irrevocable* verdict (see [6, 5] for details).

Instrumentation lies at the core of runtime monitoring [70, 22, 64]. It is the mechanism by which runtime information from a SuS is extracted and reported to monitors as a stream of system events called a *trace*. Software is typically instrumented in one of two ways. Inline instrumentation, or *inlining*, modifies the SuS by injecting tracing instructions at specific joinpoints, e.g. using AspectJ [90] or BCEL [54]. Outline instrumentation, or *outlining*, uses an external tracing infrastructure to gather events, e.g. LTTng [56] or OpenJ9 [58], thereby treating the SuS as a *black box*. A key requirement setting RV apart from monitoring, e.g., telemetry [85] or profiling [121, 26], is that the instrumentation must report *sound traces*.

▶ **Definition 1** (Sound traces). *A finite trace T is* sound *w.r.t. a system component P iff it is*

1. Complete. *T contains* all *the events exhibited by P so far,* and
2. Consistent. *The event sequence in T reflects the order the events occur* locally *at P.* ⌟

Traces violating this soundness invariant are unfit for RV, as omitted, spurious, or out-of-sequence events incorrectly characterise the system behaviour, *nullifying* the verdicts that monitors flag [22, 52]. Reactive software imposes another requirement: that the instrumentation *safeguards* the responsive, resilient, message-driven, and elastic attributes of the SuS. This necessitates an instrumentation method which is itself *reactive*, in order to

1. not hamper the SuS by inducing unfeasible runtime overhead (is responsive),
2. permit monitors to fail independently of SuS components (is resilient),
3. react to trace events without blocking the SuS (is message-driven), and
4. grow and shrink in proportion to the size of the SuS (is elastic).

Limitations of current RV instrumentation methods. State-of-the-art RV tools use instrumentation methods that do not satisfy *all* of the conditions $1-4$ above. This renders them inapplicable to reactive software; see [64, tables 3 and 4] for details. Many approaches, including [24, 31, 49, 75, 110, 122, 127, 19], assume systems with a *fixed* architecture where the number of components remains constant at runtime, failing to meet condition 4. Works foregoing the assumption of a fixed system size, such as [45, 91, 60, 59, 25, 31, 68, 3], inline the SuS with monitors *statically.* Inlining monitors pre-deployment inherently accommodates systems that grow and shrink (condition 4) as a by-product of the embedded monitor code that executes on the same thread of system components; see fig. 1a. This scheme, however, has shortcomings that make it less suited to reactive software. Recent studies [22, 52] observe that the lock-step execution of the SuS and monitors can impair the operation of the instrumented system, e.g. slow runtime analyses manifest as high latencies [37], and faulty monitors may break the system [69], which do not meet conditions 1 and 2 (e.g. M_Q in fig. 1a). Other works [46, 16] argue that errors, such as deadlocks or component crashes, are hard to detect since the monitoring logic shares the runtime thread of the affected component. Entwining the execution of the SuS and monitors may also diminish the scalability, performance, and resource usage efficiency of the monitored system because inlined monitor code cannot be run on separate threads [12]. Lastly, inlining is *incompatible* with unmodifiable software, such as closed-source components (e.g. R in figs. 1a – 1c), making outlining the only alternative.

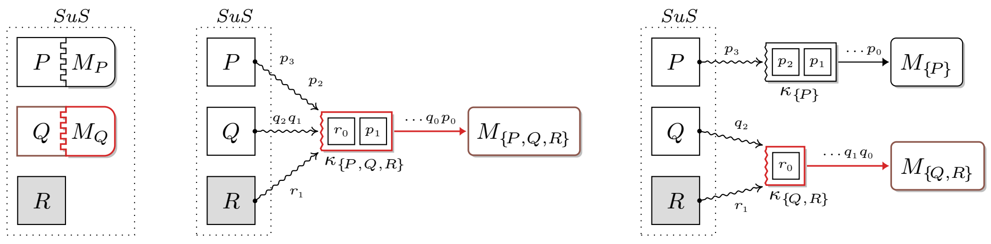
Outline instrumentation *can* address the limitations of inlining by isolating the SuS and its monitors (works [45, 37, 38] that view externalised monitors as "outline" embed tracing code to extract events from the SuS, subjecting them to the cons of inlining). The latest survey on decentralised RV [71, tables 1 and 2] establishes that outlining-based tools, e.g. [50, 18, 19, 72, 37, 38, 125, 65], are variations on *centralised* instrumentation. In this set-up, events exhibited by SuS components are funnelled through a *global* trace buffer (e.g. $\kappa_{\{P,Q,R\}}$ in fig. 1b) that a singleton monitor can analyse asynchronously, meeting condition 3. Yet, the central buffer introduces contention and sacrifices the scalability of the SuS [11], violating condition 4. Centralised architectures are prone to single point of failures (SPOFs) [94, 93] (violating condition 2), which is not ideal for monitoring medium-scale reactive systems.

Contribution. We propose RIARC, a *decentralised* instrumentation algorithm for outline monitors that overcomes the above shortcomings, fulfilling conditions 1 – 4. Outline monitors minimise latency effects due to slow trace event analyses associated with inlining (meeting condition 1). While RIARC does not handle monitor failure explicitly, it intrinsically enjoys a degree of fault tolerance by isolating the SuS and its decentralised monitor components (meeting condition 2); e.g. monitors $M_{\{P\}}$ and $M_{\{Q,R\}}$ in fig. 1c. RIARC uses a tracing infrastructure to obtain system events passively without modifying the SuS (meeting condition 3). The algorithm equips each isolated monitor with a *local* trace buffer, using it to report events based on the SuS components a monitor is tasked to analyse (e.g. buffers $\kappa_{\{P\}}$ and $\kappa_{\{Q,R\}}$ in fig. 1c). RIARC reorganises its instrumentation set-up to reflect dynamic changes in the SuS. It reacts to specific events in traces to instrument monitors for new SuS components and to remove redundant monitors when it detects graceful or abnormal component terminations. This enables RIARC to grow and shrink the verification set-up on demand (meeting condition 4). Given the challenges of fulfilling the conditions 1 – 4, we scope our work to settings where communication is reliable (i.e., no message corruption, duplication, and loss) [57] and Byzantine failures do not arise [96].

To the best of our knowledge, the approach RIARC advocates is novel. One reason why outlining has never been adopted for decentralising monitors are the onerous conditions 1 – 4 imposed by reactive software. Utilising non-invasive tracing makes our set-up necessarily *asynchronous*. At the same time, this complicates the instrumentation, which must ensure trace soundness (def. 1), notwithstanding the inherent phenomena arising from the concurrent execution of the SuS and monitors, e.g. trace event reordering and process crashes. Consequently, the second reason is that the overhead incurred to uphold this invariant – in addition to scaling the verification set-up as the SuS executes – is perceived as prohibitive when compared to inlining. This opinion is often reinforced when the viability of outline instrumentation is predicated on empirical criteria tied to monolithic, batch-style programs, that *may not* apply to reactive software (e.g. percentage slowdown); e.g. see [97, 114, 113, 47, 46, 119, 30, 98].

This paper shows how instrumenting outline monitors under conditions 1 – 4 can be achieved using a decentralised approach that guarantees def. 1, while *also* exhibiting overheads considered feasible for typical soft real-time reactive systems. Concretely, we

- **(i)** recall the benefits of the actor model [82, 10] for building reactive systems and argue how our model of processes and tracers readily maps to that setting, sec. 2;
- **(ii)** give a decentralised instrumentation algorithm for outline monitors, detailing how the reactive characteristics of the SuS can be preserved whilst ensuring def. 1, sec. 3;
- **(iii)** show the implementability of our algorithm in an actor language and systematically validate the correctness of its corresponding implementation w.r.t. def. 1 by exhaustively inducing interleaved executions for a selection of instrumented systems, sec. 4;



(a) M_Q fails, Q fails **(b)** Bottleneck or SPOF at $\kappa_{\{P,Q,R\}}$ **(c)** $\kappa_{\{Q,R\}}$ fails, $\{Q,R\}$ are unaffected

Figure 1 P,Q,R instrumented in inline (*left*), centralised (*middle*) and decentralised (*right*) modes.

(iv) back up the feasibility of the implemented algorithm via a comprehensive empirical study that uses various workload configurations surpassing the state of the art, showing that the induced overhead minimally impacts the reactive attributes of the SuS, sec. 5.

The extended version [8] contains the full details about RIARC and further discussion of our experiments and results. That material is ancillary to the one presented in this paper.

2 A computational model for reactive systems

The actor model [82, 10] emerged as *the* paradigm to design and build reactive systems [33]. *Actors* – the units of decomposition in this model – are abstractions of concurrent entities that share no mutable memory with other actors. Instead, actors interact through asynchronous message passing and alter their internal state based on the messages they consume. Asynchronous communication decouples actors spatially and temporally, which fully isolates system components and establishes the foundation for resiliency and elasticity [32, 94]. Each actor is equipped with an incoming message buffer called the *mailbox*, from which messages deposited by other actors can be selectively read. Besides sending and receiving messages, actors can *spawn* other actors. Actors in a system are addressable by their unique process identifier (PID), which they use to engage in directed, *point-to-point* communication. This idea of addressability is central to the actor model: it enables reasoning about decentralised computation, as the identity of components or messages can be propagated through a system and used in handling complex tasks, such as process registration and failure recovery [33]. As is often the case in decentralised computations, we assume that messages exchanged between pairs of processes are always received in the order in which they have been sent [43].

Frameworks, notably Erlang [12], Elixir [88], Akka [1] for Scala [117], along with others [118, 130], instantiate the actor model. We adopt Erlang since its ecosystem is specifically engineered for highly-concurrent, soft real-time reactive systems [131, 13, 44]. The Erlang virtual machine (EVM) implements actors as lightweight processes. It employs *per process* garbage collection that, unlike the JVM, does not subject the virtual machine to global unpredictable pauses [86, 116]. This factor minimises the impact on the soft real-time properties of a system *and* is also crucial to the empirical evaluation of sec. 5 since it stabilises the variance in our experiments. The EVM exposes a flexible *process tracing* API aimed at reactive software [42]. Erlang provides other components, e.g. supervision trees, message queues, etc., for building fault-tolerant distributed applications. While we scope our work to fault-free settings (see sec. 1), adopting Erlang gives us the foundation upon which our work can be naturally extended to address these aspects. Henceforth, we follow the established convention in Erlang literature and use the terms *actor*, *process*, and *component* synonymously.

2.1 Process tracing and trace partitioning

Processes in a concurrent system form a *tree*, starting at the *root* process that spawns *child* processes, and so forth[1]. Concurrency induces inherent *partitions* to the execution of the SuS in the form of isolated traces that reflect the *local* behaviour at each process [19]. RIARC exploits this aspect to attain several benefits. First, one can *selectively* specify the SuS processes to be instrumented. The upshot is that fewer trace events need to be gathered, improving *efficiency*. Another benefit of partitioned traces is that each process can be dynamically instrumented, free from assumptions about the number of processes the SuS is expected to have. This makes the RV set-up *elastic*. Lastly, the instrumentation set-up can *partially fail*, as faulty SuS or monitor processes do not imperil the execution of one another.

▶ **Example 2** (Trace partitions). Trace partitions enable RIARC to instrument a system in various arrangements. Fig. 2a depicts an interaction sequence for the execution of the SuS from sec. 1. In this interaction, the root process, P, spawns Q and communicates with it, at which point Q spawns process R; P and Q eventually terminate. We denote the process *spawning* and *termination* trace events by $-\!\!\diamond$ and $\ast$, and use $!$ and $?$ for *send* and *receive* events respectively. The *sound* trace partitions for the processes in fig. 2a are “$-\!\!\diamond_P.!_P.\ast_P$” for P, “$?_Q.-\!\!\diamond_Q.\ast_Q$” for Q, and the empty trace for R. ⌟

A centralised set-up such as that of fig. 1b can be obtained by instrumenting $\{P,Q,R\}$ with one monitor, $M_{\{P,Q,R\}}$, whereas instrumenting the components $\{P\}$ and $\{Q,R\}$ with monitors $M_{\{P\}}$ and $M_{\{Q,R\}}$ gives the decentralised arrangement of fig. 1c. Each of these instrumentation arrangements generates different executions.

▶ **Example 3** (Sound traces). For the case of fig. 1b, RIARC can report to $M_{\{P,Q,R\}}$ *one* of four possible traces “$-\!\!\diamond_P.!_P.\ast_P.?_Q.-\!\!\diamond_Q.\ast_Q$”, “$-\!\!\diamond_P.!_P.?_Q.\ast_P.-\!\!\diamond_Q.\ast_Q$”, “$-\!\!\diamond_P.!_P.?_Q.-\!\!\diamond_Q.\ast_P.\ast_Q$”, or “$-\!\!\diamond_P.!_P.?_Q.-\!\!\diamond_Q.\ast_Q.\ast_P$”. These *sound* traces result from the interleaved execution of processes P, Q. Any other trace, e.g. “$-\!\!\diamond_P.\ast_P.?_Q.-\!\!\diamond_Q.\ast_Q$” or “$-\!\!\diamond_P.!_P.\ast_P.?_Q.\ast_Q.-\!\!\diamond_Q$”, is *unsound* since it contradicts the local behaviour at processes P and Q of fig. 2a. The former trace omits the request $!_P$ that P makes to Q (it is *incomplete* w.r.t. P), and the latter trace inverts $-\!\!\diamond_Q$ and $\ast_Q$, suggesting that Q spawns R after Q terminates (it is *inconsistent* w.r.t. Q). ⌟

▶ **Example 4** (Separate instrumentation). Fig. 2b shows another decentralised set-up, where P, Q, and R are instrumented separately. In this case, the instrumentation should report to $M_{\{P\}}$, $M_{\{Q\}}$ and $M_{\{R\}}$ the events observed *locally* at each process, as stated in ex. 2. ⌟

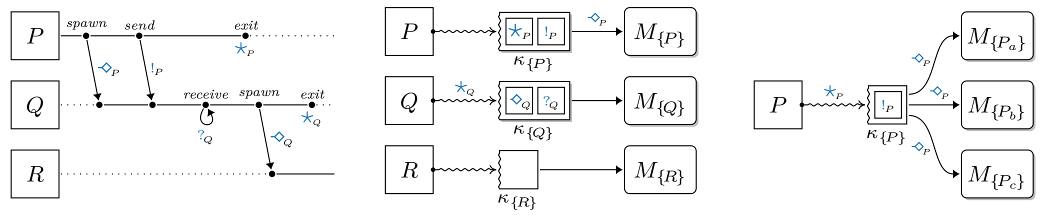
RIARC makes two assumptions about process tracing in order to support the instrumentation arrangements shown in figs. 1b, 1c, and 2b:

A$_1$ *Tracing processes sets.* Tracing can gather events for *sets* of SuS processes, e.g. $\kappa_{\{P,Q,R\}}$ in fig. 1b gathers the events of $\{P,Q,R\}$, and $\kappa_{\{Q,R\}}$ in fig. 1c gathers the events of $\{Q,R\}$.

A$_2$ *Tracing inheritance.* Tracing gathers the events of a SuS process *and* the children it spawns by default to eliminate the risk that trace events from child processes are missed.

We opt for tracing inheritance since it follows established centralised RV monitoring tools, including [18, 41, 50, 110]. In fact, tracing assumptions A$_1$ and A$_2$ mean that centralised set-ups like that of fig. 1b can be obtained just by tracing the root process P. Tracing inheritance requires the instrumentation to *intervene* if it needs to channel the events of a child process into a *new* trace partition that is *independent* from that of its parent, e.g. as in

[1] For example, using `spawn()` in Erlang [42] and Elixir [88], `ActorContext.spawn()` in Akka [1], `Actor.createActor()` in Thespian [118], `CreateProcess()` in Windows [108], etc.



(a) Interaction flow of P, Q and R. **(b)** Trace partitions of P, Q, and R. **(c)** Event replicas to monitors.

Figure 2 SuS with processes P, Q, and R instrumented with independent monitors.

fig. 1c. In such cases, the instrumentation must first stop tracing the child process, allocate a fresh trace buffer, and resume tracing the child process. The out-of-sync execution of the SuS and instrumentation complicates the creation of these new trace partitions because it can lead to reordered or missed events. This, in turn, would violate trace soundness, def. 1.

We supplement A_1 and A_2 with the following to keep our exposition in sec. 3 manageable:

A$_3$ *Single-process tracing.* Any SuS process can be traced *at most* once at any point in time.

A$_4$ *Causally-ordered spawn events.* Tracing gathers the spawn trace event of a parent process before *all* the events of the child process spawned by that parent, e.g. if P spawns Q, and Q receives, as in fig. 2a, the reported sequence is "$\multimap_P . ?_Q$" rather than "$?_Q . \multimap_P$".

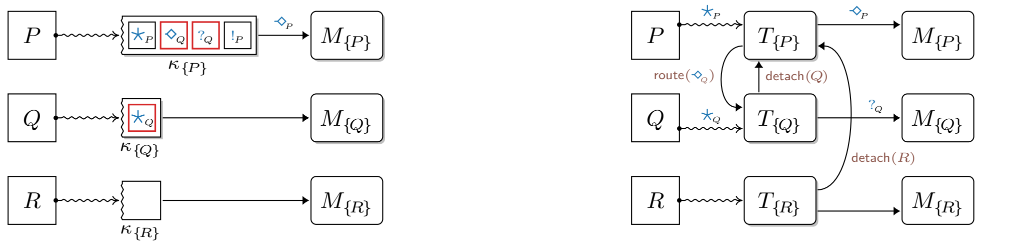
The constraint of tracing assumption A_3 is easily overcome by replicating trace events for a process and reporting them to different monitors (e.g. the events in the trace partition of process P are replicated to monitors $M_{\{P_a\}}$, $M_{\{P_b\}}$, $M_{\{P_c\}}$ in fig. 2c). Tracing assumption A_4 requires trace buffers to reorder $\multimap$ events using the spawner and spawned process information carried by each event before reporting them to monitors. Sec. 3.3 gives more details.

▶ **Example 5** (Unsound traces). Fig. 3a shows one possible configuration that can be reached by our three-process system introduced in fig. 2a, where the trace buffer $\kappa_{\{P\}}$ contains the events for both P and Q. The trace in buffer $\kappa_{\{Q\}}$ is unsound, as it inaccurately characterises the local behaviour of process Q (the sound trace for Q should be "$?_Q . \multimap_Q . \ast_Q$", not "$\ast_Q$"). ⌟

RIARC programs trace buffers to coordinate with one another to ensure that sound traces are invariably reported to monitors. We refer to a trace buffer and the coordination logic it encapsulates as a *tracer*. RIARC employs an approach based on *next-hop routing* in IP networks [80, 104] to counteract the effects of trace event reordering and loss by rearranging and forwarding events to different tracers. Fig. 3b conveys our organisation of tracers (refer to [8, fig. 10 in app. A] for legend). Sec. 3 details how RIARC dynamically reorganises the tracer choreography and performs next-hop routing.

2.2 Modelling decentralised instrumentation

Since RV monitors are passive verdict-flagging machines (refer to sec. 1), they are orthogonal to our instrumentation. We, thus, focus our narrative on tracers and omit monitors, except when relevant in the surrounding context. The model assumes a set of SuS process, $P, Q, R \in \textsc{Prc}$, and tracer names, $T \in \textsc{Trc}$, together with a countable set of PID values to reference processes. We distinguish between SuS and tracer PIDs, which we denote respectively by the sets, $p_{\text{s}}, q_{\text{s}} \in \textsc{Pid}_{\text{s}}$ and $p_{\text{T}}, q_{\text{T}} \in \textsc{Pid}_{\text{T}}$. The variables $\imath_{\text{s}}$ and $\jmath_{\text{s}}$, and $\imath_{\text{T}}$ and $\jmath_{\text{T}}$ range over PIDs from the corresponding sets $\textsc{Pid}_{\text{s}}$ and $\textsc{Pid}_{\text{T}}$. We also assume the function signature sets, $f_{\text{s}} \in \textsc{Sig}_{\text{S}}$, $f_{\text{T}} \in \textsc{Sig}_{\text{T}}$, and, $f_{\text{M}} \in \textsc{Sig}_{\text{M}}$, to denote SuS, tracer, and RV monitor functions, together with



(a) Buffer $\kappa_{\{Q\}}$ missing trace prefix "$?_Q . \multimap_Q$" **(b)** Coordinating tracers $T_{\{P\}}$, $T_{\{Q\}}$, and $T_{\{R\}}$

Figure 3 Choreographed tracers coordinating to ensure sound traces.

the variables ς_S, ς_T, and ς_M that range over each signature set. New SuS processes are created via the function $\mathsf{spwn}(\varsigma_S)$ that accepts the function signature ς_S to be spawned, and returns a fresh PID, $\imath_S$. We overload spwn to spawn tracer signatures ς_T equivalently, returning corresponding PIDs, $\imath_T$. The function self obtains the PID of the process invoking it. We write P as shorthand for a singleton process set $\{P\}$ to simplify notation.

RIARC uses three message types, $\tau \in \{\mathsf{evt}, \mathsf{dtc}, \mathsf{rtd}\}$. These determine when to *create* or *terminate* tracer processes, and what trace events to *route* between tracers:

- evt are *trace events* gathered via process tracing,
- dtc are *detach* requests that tracers exchange to reorganise the tracer choreography, and
- rtd are *routing* packets that transport evt or dtc messages forwarded between tracers.

We encode messages m as tuples. Trace event messages, $\langle \mathsf{evt}, \ell, \imath_S, \jmath_S, \varsigma_S \rangle$, comprise the event label ℓ that ranges over the SuS events $\multimap$ *(spawn)*, $\ast$ *(exit)*, ! *(send)*, and ? *(receive)*. The PID value $\imath_S$ identifies the SuS process exhibiting the trace event, and is defined for *all* events. The SuS PID $\jmath_S$ and function signature ς_S depend on the type of the event. Tbl. 1a catalogues the values defined for each event. We write trace events in their shorthand form, omitting undefined values (denoted by $\perp$), e.g. $\langle \mathsf{evt}, \ast, \imath_S \rangle$ instead of $\langle \mathsf{evt}, \ast, \imath_S, \perp, \perp \rangle$.

Table 1 Trace event (evt), detach request (dtc), and routing packet (rtd) message index names.

(a) Messages encoding *spawn*, *exit*, *send*, and *receive* events.

Label ℓ	Index	Description ($\imath_S$ and $\jmath_S$ are SuS PIDs)
$\multimap$	$e.\imath_S$	Parent PID spawning new child PID $\jmath_S$
	$e.\jmath_S$	Child PID spawned by parent PID $\imath_S$
	$e.\varsigma_S$	Signature ς_S spawned by parent PID $\imath_S$
$\ast$	$e.\imath_S$	Terminated PID
	$e.\jmath_S, e.\varsigma_S$	*Undefined for exit events*
!	$e.\imath_S$	Sending PID
	$e.\jmath_S$	Recipient PID
	$e.\varsigma_S$	*Undefined for send events*
?	$e.\imath_S$	Recipient PID
	$e.\jmath_S, e.\varsigma_S$	*Undefined for receive events*

(b) Detach and routing messages.

Index	Description
$m.\tau$	Message type: event (evt) detach (dtc), routing (rtd)
$d.\imath_T$	PID of tracer requesting detach of SuS PID $\imath_S$
$d.\imath_S$	PID of SuS process to stop tracing
$r.\imath_T$	PID of tracer that starts routing message m
$r.m$	Embedded evt or dtc message being routed

Table 2 RIARC approach to ensure trace soundness (def. 1) and reactive instrumentation (sec. 1).

Requirement	Approach
R_1 Growing the set-up	Instrument tracers on-demand to create new trace partitions
R_2 Ensuring complete traces	Route trace events to deliver them to the correct tracer
R_3 Ensuring consistent traces	Prioritise routed trace events before others
R_4 Isolating tracers	Detach tracers from others once all trace events are routed
R_5 Minimising overhead	Target specific processes to instrument
R_6 Shrinking the set-up	Garbage collect redundant tracers and monitors

Detach request messages have the form $\langle \mathsf{dtc}, \imath_T, \imath_S \rangle$. A tracer with the PID $\imath_T$ uses dtc to request that another tracer *stop* tracing the SuS PID $\imath_S$. Routing packet messages, $\langle \mathsf{rtd}, \imath_T, m \rangle$, move evt and dtc messages between tracers. The PID $\imath_T$ identifies the tracer that embeds the message m into the routing packet and dispatches it to other tracers. Tbl. 1b summarises detach request and routing packet messages.

▶ Note 6 (Notation). We reserve the variables e, d, and r for the messages types evt, dtc, and rtd respectively. Our model uses the suggestive dot notation (.) to index message fields, e.g. $m.\tau$ reads the message type, $e.\ell$ reads the trace event label, etc. (see tbl. 1). For simplicity, we occasionally write the label ℓ in lieu of the full trace event form, e.g. we write $\star$ instead of $\langle \mathsf{evt}, \star, \imath_S \rangle$, etc. ⌟

3 Decentralised instrumentation

Our reason for encapsulating trace buffers and their coordination logic as tracers stems from the actor model. Trace buffers align with actor mailboxes, which localise the tracer state and enable tracers to run *independently*. The main logic replicated at each tracer is given in algs. 1 – 3. Tracers operate in two modes, *direct* (○) and *priority* (●), to counteract the effects of trace event reordering. We organise our tracer logic in algs. 1 and 3 to reflect these modes, respectively. Algs. 1 and 3 use the function AnalyseEvt, which analyses events; see [8, app. C.5.2] for details. Auxiliary tracer logic referenced in this section is given in [8, app. A].

Every tracer maintains an internal state σ consisting of the following three maps:

- the *routing* map, Π, governing how events are routed to other tracers,
- the *instrumentation* map, Λ, that determines which SuS processes to instrument, and
- the *traced-processes* map, Γ, tracking the SuS process set that the tracer currently traces.

Tbl. 2 summarises the challenges that RIARC needs to overcome to attain the reactive characteristics stated in sec. 1. Requirements R_1 and R_6 in tbl. 2 oblige the instrumentation to reorganise dynamically while the SuS executes to preserve its *elasticity*. Requirement R_4 offers a modicum of *resiliency* between the SuS and tracer processes, whereas R_5 minimises the instrumentation overhead by gathering only the events monitors require. This keeps the overall set-up *responsive*. Since RIARC builds on the actor model, it fulfils the *message-driven* requirement intrinsically. *Trace soundness* is safeguarded by requirements R_2 and R_3.

The operations Trace, Clear and Preempt give access to the tracing infrastructure. Trace($\imath_S$,$\imath_T$) enables a tracer with PID $\imath_T$ to register its interest in receiving trace events of a SuS process with PID $\imath_S$. This operation can be undone using Clear($\imath_S$,$\imath_T$), which *blocks* the calling tracer $\imath_T$ and returns once all the trace event messages for the SuS process $\imath_S$ that are in transit to the tracer $\imath_T$ have been delivered to $\imath_T$. It is worth remarking that this behaviour conforms to our proviso in sec. 1, i.e., no communication faults. Preempt($\imath_S$,$\imath_T$) combines

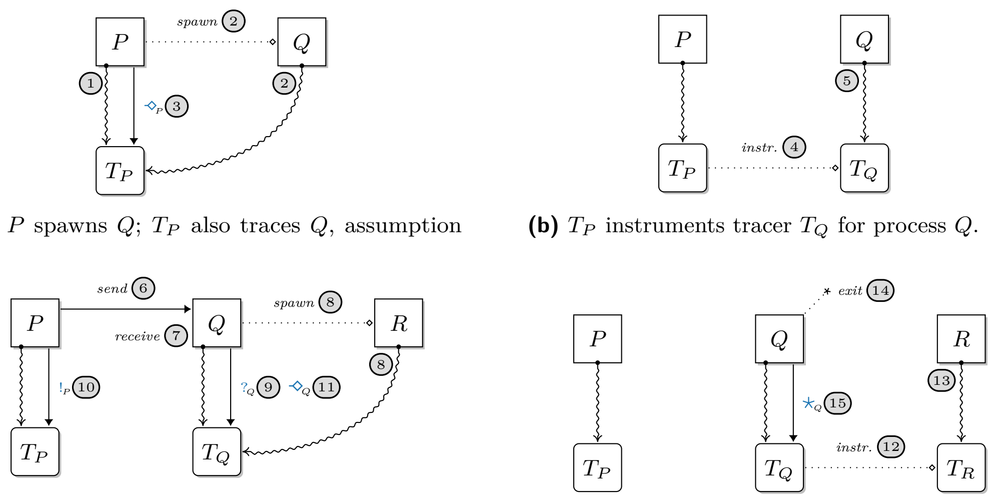
Clear and Trace. It enables the tracer pre-empting $\imath_{\text{T}}$ to take control of tracing the SuS process $\imath_{\text{S}}$ from another tracer $\imath'_{\text{T}}$ that is currently tracing $\imath_{\text{S}}$. Tracers use Clear or Preempt to modify the default process-tracing inheritance behaviour that tracing assumption A_2 describes. We refer readers to [8, alg. 5 in app. A] for the specifics of these operations.

We focus our presentation in secs. 3.1 – 3.6 of how RIARC addresses the challenges listed in tbl. 2 on the set-up of fig. 2b, where the processes P, Q and R, are instrumented separately. This specific case highlights two aspects. First, it *emphasises* the complications that RIARC overcomes to establish the desired set-up while ensuring trace soundness, def. 1. Second, fig. 2b *covers all* other possible instrumentation set-ups. Disjoint sets of SuS processes, including the one shown in fig. 1c, can be obtained when tracers do not act on certain -◇ (*spawn*) events, as sec. 3.1 explains. Notably, *any* centralised set-up, e.g. the one in fig. 1b, emerges naturally when the root tracer disregards all -◇ events exhibited by the SuS.

▶ Note 7 (Naming conventions). For clarity, we adopt the convention that a SuS process P is spawned from the signature f_{S_P} and is assigned the PID p_{S}. A tracer for P is named T_P (short for $T_{\{P\}}$) and has the PID p_{T}. Other processes are treated likewise, e.g. the SuS process Q has signature f_{S_Q}, PID q_{S}, while the tracer T_Q for Q has PID q_{T}, etc. ⌟

3.1 Growing the set-up

Fig. 4 illustrates how the hierarchical creation sequence of SuS processes described in sec. 2.1 is exploited to instrument separate tracers. RIARC programs tracers to react to -◇ (*spawn*) events in the trace. In fig. 4a, the root tracer T_P traces process P, step ①. When P spawns process Q, Q automatically inherits T_P (tracing assumption A_2 from sec. 2.1). Steps ② in fig. 4a emphasise that tracing inheritance is instantaneous. The event $e = \langle \mathsf{evt}, \text{-}\!\diamond, p_{\text{S}}, q_{\text{S}}, f_{\text{S}_Q} \rangle$ is generated by P when it spawns its child Q, step ③ in fig. 4a. The PID values of the parent and child processes carried by e, namely p_{S} and q_{S}, are accessed via the indexes $e.\imath_{\text{S}}$ and $e.\jmath_{\text{S}}$ respectively (see tbl. 1a). Tracer T_P uses this PID information to instrument a new tracer T_Q for process Q in step ④ of fig. 4b. By invoking Preempt(q_{S},q_{T}), T_Q takes over tracing process Q from the former tracer T_P going forward. T_Q creates a new trace partition for



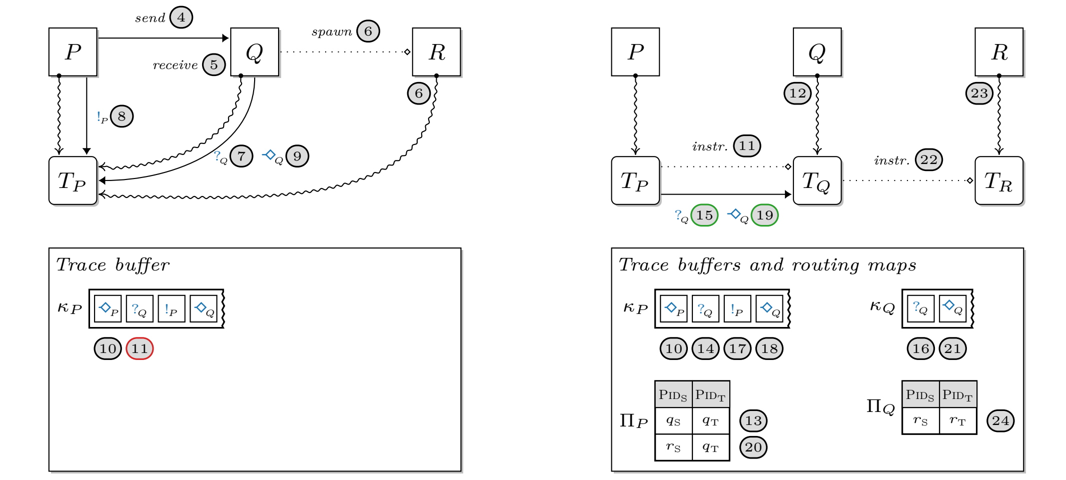
(a) P spawns Q; T_P also traces Q, assumption A_2.

(b) T_P instruments tracer T_Q for process Q.

(c) T_P and T_Q analyse trace events separately.

(d) P, Q, R and corresponding tracers.

Figure 4 Growing the tracer instrumentation set-up for processes P, Q and R (monitors omitted).



(a) Trace events for P, Q, and R received by T_P. **(b)** Trace events for Q routed from T_P to T_Q.

Figure 5 Next-hop trace event routing using tracer routing maps Π (monitors omitted).

process Q that is independent of the partition of P, step ⑤. Meanwhile, T_P receives the send event $\langle \mathsf{evt}, !, p_{\mathrm{S}}, q_{\mathrm{S}} \rangle$ in step ⑩ after P messages Q in step ⑥ of fig. 4c. Subsequent $\multimap$ events that T_P or T_Q may gather are handled as described in steps ③–⑤. Figs. 4c and 4d show how the final tracer T_R is instrumented in step ⑫ after Q spawns R in step ⑧. As before, T_Q traces R automatically in step ⑧. T_Q receives the event $\langle \mathsf{evt}, \multimap, q_{\mathrm{S}}, r_{\mathrm{S}}, f_{\mathrm{S}_R} \rangle$ generated by Q in step ⑪. T_R invokes Preempt$(r_{\mathrm{S}}, r_{\mathrm{T}})$ to create the trace partition for R in step ⑬.

3.2 Ensuring complete traces

The asynchrony between the SuS and tracer processes can induce the interleaved execution shown in fig. 5, as an alternative execution to that shown in figs. 4b–4d. In fig. 5a, T_P is slow to handle $\multimap_P$ it receives in ③ of fig. 4a and fails to instrument T_Q promptly. Consequently, the events $?_Q$ and $\multimap_Q$ that Q exhibits are sent to T_P in steps ⑦ and ⑨ of fig. 5a. Step ⑪ shows the case where $\langle \mathsf{evt}, ?, q_{\mathrm{T}} \rangle$ is processed by T_P, rather than by the *intended* tracer T_Q that would have been instrumented by T_P. This error breaches the *completeness* property of trace soundness w.r.t. Q, as the events $?_Q$ and $\multimap_Q$ meant for Q reach the wrong tracer T_P.

To address this issue, RIARC uses a next-hop routing approach, where tracers *retain* the events they should handle and *forward* the rest to neighbouring tracers. We use the term *dispatch tracer* (*dispatcher* for short) to describe a tracer that receives trace events meant to be handled by another tracer. For instance, T_P in fig. 5a becomes the dispatch tracer for Q when it receives the events $?_Q$ and $\multimap_Q$ exhibited by Q, steps ⑦ and ⑨. We expect these events to be handled by T_Q once it is instrumented. Dispatchers are tasked with embedding trace event (evt) or detach requests (dtc) into routing packet messages (rtd) and transmitting them to the next *known* hop. In fig. 5b, T_P dispatches the events $?_Q$ and $\multimap_Q$ as follows. It first instruments T_Q with Q in step ⑪. Next, T_P prepares $\langle \mathsf{evt}, ?, r_{\mathrm{S}} \rangle$ and $\langle \mathsf{evt}, \multimap, q_{\mathrm{S}}, r_{\mathrm{S}}, f_{\mathrm{S}_R} \rangle$ for transmission by embedding each in rtd messages (steps ⑭ and ⑱). T_P forwards the resulting routing packets, $\langle \mathsf{rtd}, p_{\mathrm{T}}, \langle \mathsf{evt}, ?, r_{\mathrm{S}} \rangle \rangle$ and $\langle \mathsf{rtd}, p_{\mathrm{T}}, \langle \mathsf{evt}, \multimap, q_{\mathrm{S}}, r_{\mathrm{S}}, f_{\mathrm{S}_R} \rangle \rangle$, to its next-hop neighbour T_Q in steps ⑮ and ⑲. The trace event $\langle \mathsf{evt}, !, p_{\mathrm{S}}, q_{\mathrm{S}} \rangle$, however, is not forwarded but handled by T_P, as step ⑰ shows. Concurrently, T_Q acts on the forwarded events $?_Q$ and $\multimap_Q$ in steps ⑯ and ㉑ and instruments T_R as a result, step ㉒.

Algorithm 1 Logic handling $\circ$ trace events, detach request dispatching, and forwarding.

```
1  def Loop∘($\sigma$,$\varsigma_M$)
2    forever do
3      $m \leftarrow$ next message from trace buffer $\kappa$
4      match $m.\tau$ do
5        case evt : $\sigma \leftarrow$ HandlEvent∘($\sigma$,$\varsigma_M$,$m$)
6        case dtc : $\sigma \leftarrow$ DispatchDtc($\sigma$,$\varsigma_M$,$m$)
7        case rtd : $\sigma \leftarrow$ ForwdRtd∘($\sigma$,$\varsigma_M$,$m$)

8  def HandlEvt∘($\sigma$,$\varsigma_M$,$e$)
9    match $e.\ell$ do
10     case -◇ : return HandlSpwn∘($\sigma$,$\varsigma_M$,$e$)
11     case ✻ : return HandlExit∘($\sigma$,$\varsigma_M$,$e$)
12     case !,? : return HandlComm∘($\sigma$,$\varsigma_M$,$e$)

13 def HandlSpwn∘($\sigma$,$\varsigma_M$,$e$)
14   match $\sigma.\Pi(e.\imath_S)$ do
15     case $\perp$ : # No next-hop for $e.\imath_S$; handle $e$
16       AnalyseEvt($\varsigma_M$,$e$)
17       $\sigma \leftarrow$ Instrument∘($\sigma$,$e$,self())
18     case $\jmath_T$ : # Next-hop for $e.\imath_S$ exists via $\jmath_T$
19       Dispatch($e$,$\jmath_T$)
         # Set next-hop of $e.\jmath_S$ to tracer of $e.\imath_S$
20       $\sigma.\Pi \leftarrow \sigma.\Pi \cup \{\langle e.\jmath_S, \jmath_T\rangle\}$
21   return $\sigma$

22 def HandlExit∘($\sigma$,$\varsigma_M$,$e$)
23   match $\sigma.\Pi(e.\imath_S)$ do
24     case $\perp$ : # No next-hop for $e.\imath_S$; handle $e$
25       AnalyseEvt($\varsigma_M$,$e$)
26       $\sigma.\Gamma \leftarrow \sigma.\Gamma \setminus \{\langle e.\imath_S, \circ\rangle\}$
27       TryGC($\sigma$)
28     case $\jmath_T$ : Dispatch($e$,$\jmath_T$)
29   return $\sigma$

30 def HandlComm∘($\sigma$,$\varsigma_M$,$e$)
31   match $\sigma.\Pi(e.\imath_S)$ do
32     case $\perp$ : AnalyseEvt($\varsigma_M$,$e$)
33     case $\jmath_T$ : Dispatch($e$,$\jmath_T$)
34   return $\sigma$

35 def DispatchDtc($\sigma$,$d$)
36   match $\sigma.\Pi(d.\imath_S)$ do
37     case $\perp$ : fail dtc next-hop must be defined
38     case $\jmath_T$ :
39       Dispatch($d$,$\jmath_T$)
         # Next-hop for $d.\imath_S$ no longer needed
40       $\sigma.\Pi \leftarrow \sigma.\Pi \setminus \{\langle d.\imath_S, \jmath_T\rangle\}$
41       TryGC($\sigma$)
42   return $\sigma$

43 def ForwdRtd∘($\sigma$,$r$)
44   $m \leftarrow r.m$ # Read embedded message in $r$
45   match $m.\tau$ do
46     case dtc : return ForwdDtc($\sigma$,$r$)
47     case evt : return ForwdEvt($\sigma$,$r$)

48 def ForwdDtc($\sigma$,$r$)
49   $d \leftarrow r.m$
50   match $\sigma.\Pi(d.\imath_S)$ do
51     case $\perp$ : fail dtc next-hop must be defined
52     case $\jmath_T$ :
53       Forwd($r$,$\jmath_T$)
         # Next-hop for $d.\imath_S$ no longer needed
54       $\sigma.\Pi \leftarrow \sigma.\Pi \setminus \{\langle d.\imath_S, \jmath_T\rangle\}$
55       TryGC($\sigma$)
56   return $\sigma$

57 def ForwdEvt($\sigma$,$r$)
58   $e \leftarrow r.m$
59   match $\sigma.\Pi(e.\imath_S)$ do
60     case $\perp$ : fail evt next-hop must be defined
61     case $\jmath_T$ :
62       Forwd($r$,$\jmath_T$)
         # For spawn events, tracer also sets a
         # new next-hop for $e.\jmath_S$
         # Next-hop of $e.\jmath_S$ to same tracer of $e.\imath_S$
63       if ($e.\ell$ = -◇)
64         $\sigma.\Pi \leftarrow \sigma.\Pi \cup \{\langle e.\jmath_S, \jmath_T\rangle\}$
65   return $\sigma$
```

Tracers determine the events to retain or forward using the routing map, $\Pi : \mathrm{PID_S} \rightharpoonup \mathrm{PID_T}$. Every tracer queries its private routing map for each message it receives on SuS PID $m.\imath_S$. A tracer forwards a message to its neighbouring tracer with PID $\imath_T$ if a next-hop for that message exists, i.e., $\Pi(m.\imath_S) = \imath_T$. When the next-hop is undefined, i.e., $\Pi(m.\imath_S) = \perp$, m is handled by the tracer. HandlSpwn, HandlExit and HandlComm in alg. 1 implement this forwarding logic on lines 14, 23 and 31.

Dynamically populating the routing map is key to transmitting messages between tracers. A tracer adds the new mapping $e.\jmath_S \mapsto \jmath_T$ to its routing map Π in case 1 or 2 below whenever it processes spawn trace events $e = \langle \mathsf{evt}, \text{-}\!\diamond, \imath_S, \jmath_S, \varsigma_S\rangle$. One of two cases is considered for $e.\imath_S$:

Algorithm 2 Tracer instrumentation operations for direct (∘) and priority (•) modes.

```
Expect: $e = \langle \mathsf{evt}, {-\!\!\diamond}, \imath_S, \jmath_S, \varsigma_S \rangle$
1  def INSTRUMENT$_\circ(\sigma, e, \imath_T)$
2    if $((\varsigma_M \leftarrow \sigma.\Lambda(e.\varsigma_S)) \neq \bot)$
       # New tracer $\jmath_T$ for new SuS process $e.\jmath_S$
3      $\jmath_T \leftarrow \mathsf{spwn}(\text{TRACER}(\sigma, \varsigma_M, e.\jmath_S, \imath_T))$
4      $\sigma.\Pi \leftarrow \sigma.\Pi \cup \{\langle e.\jmath_S, \jmath_T \rangle\}$
5    else
       # In ∘ mode, this tracer has detached
       # all processes from its dispatcher $\imath_T$
       # This tracer traces new SuS process $e.\jmath_S$
       # by tracing inheritance assumption $A_2$
6      $\sigma.\Gamma \leftarrow \sigma.\Gamma \cup \{\langle e.\jmath_S, \circ \rangle\}$
7    return $\sigma$
```

```
Expect: $e = \langle \mathsf{evt}, {-\!\!\diamond}, \imath_S, \jmath_S, \varsigma_S \rangle$
8  def INSTRUMENT$_\bullet(\sigma, e, \imath_T)$
9    if $((\varsigma_M \leftarrow \sigma.\Lambda(e.\varsigma_S)) \neq \bot)$
       # New tracer $\jmath_T$ for new SuS process $e.\jmath_S$
10     $\jmath_T \leftarrow \mathsf{spwn}(\text{TRACER}(\sigma, \varsigma_M, e.\jmath_S, \imath_T))$
11     $\sigma.\Pi \leftarrow \sigma.\Pi \cup \{\langle e.\jmath_S, \jmath_T \rangle\}$
12   else
       # In • mode, this tracer must detach
       # SuS process $e.\jmath_S$ from its dispatcher $\imath_T$
13     DETACH$(e.\jmath_S, \imath_T)$
       # This tracer traces new SuS process $e.\jmath_S$
14     $\sigma.\Gamma \leftarrow \sigma.\Gamma \cup \{\langle e.\jmath_S, \bullet \rangle\}$
15   return $\sigma$
```

1. $\Pi(\imath_S) = \bot$. The next-hop for e is undefined, which cues the tracer to instrument the SuS process with PID $\jmath_S$. When applicable, the tracer processes the event *and* instruments a separate tracer with PID $\jmath_T$. It then adds the mapping $e.\jmath_S \mapsto \jmath_T$ to Π. The tracer leaves Π *unmodified* and handles the event itself if a separate tracer is not required. Opting for a separate tracer is determined by the instrumentation map Λ, as discussed in sec. 3.5.
2. $\Pi(\imath_S) = \jmath_T$. The next-hop for e is defined, and the tracer forwards the event to the neighbouring tracer $\jmath_T$. The tracer also records a new next-hop by adding $e.\jmath_S \mapsto \jmath_T$ to Π.

The addition of $e.\jmath_S \mapsto \jmath_T$ in cases 1 and 2 ensures that future events originating from $\jmath_S$ can always be forwarded via a next-hop to a neighbouring tracer $\jmath_T$ (see invariants on lines 37, 51, and 60). Fig. 5b shows the routing maps of the tracers T_P and T_Q. T_P adds $q_S \mapsto q_T$ in step ⑬ after processing $\langle \mathsf{evt}, {-\!\!\diamond}, p_S, q_S, f_{S_Q} \rangle$ from its trace buffer in ⑩. T_P then instruments Q with the tracer T_Q in step ⑪; an instance of case 1. The function INSTRUMENT in alg. 2 details this on line 4, where the mapping $e.\jmath_S \mapsto \jmath_T$ is added to Π following the creation of tracer $\jmath_T$, line 3. Step ⑳ of fig. 5b is an instance of case 2. Here, T_P adds $r_S \mapsto q_T$ to Π_P after processing $\langle \mathsf{evt}, {-\!\!\diamond}, q_S, r_S, f_{S_R} \rangle$ for R in step ⑱ since $\Pi_P(q_S) = q_T$. Crucially, T_P *does not* instrument a new tracer, but delegates the task to T_Q by forwarding ${-\!\!\diamond}_Q$. Lines 20 and 64 in alg. 1 (and later line 24 in alg. 3) are manifestations of this, where the mapping $e.\jmath_S \mapsto \jmath_T$ is added after the ${-\!\!\diamond}$ event e is forwarded to the next-hop $\jmath_T$. T_Q instruments the SuS process R in step ㉒ with T_R, which has the PID r_T. It then adds the mapping $r_S \mapsto r_T$ to Π_Q in step ㉔, as no next-hop is defined for q_S, i.e., $\Pi_Q(q_S) = \bot$. Henceforth, any events exhibited by R and received at T_P can be dispatched by the latter tracer through T_Q to T_R.

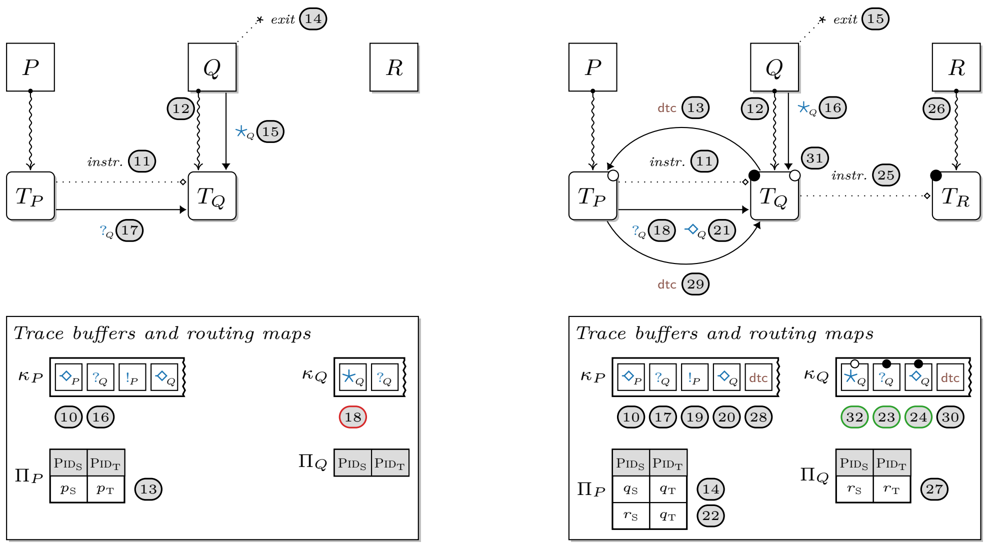
Note that every tracer is *only* aware of its neighbouring tracers. This means messages may pass through multiple tracers before reaching their intended destination. Next-hop routing keeps the logic inside RIARC straightforward since tracers forward messages based on local information in their routing map. This approach makes the instrumentation set-up adaptable to dynamic changes in the SuS and has been shown to induce lower latency when compared to general routing strategies [80, 104]. The DAG of interconnected tracers induced by next-hop routing ensures that every message is eventually delivered to the correct tracer if a path exists or handled by the tracer otherwise. Fig. 5b illustrates this concept, where the next-hop mappings inside Π_P point to T_Q, and the mappings in Π_Q point to T_R. Consequently, any events that R exhibits and that T_P receives are forwarded *twice* to reach the target tracer T_R: from tracer T_P to T_Q, and from T_Q to T_R. RIARC relies on the operations DISPATCH and FORWD to achieve next-hop routing (see [8, alg. 4 in app. A]). DISPATCH creates a routing packet, $\langle \mathsf{rtd}, \imath_T, m \rangle$, and embeds the trace event or detach message m to be routed. Alg. 1 shows how tracers handle routing packets. For instance, FORWDEVT extracts the embedded message from the routing packet on line 58 and queries the routing map to determine the next-hop, line 59. If found, the packet is forwarded, as FORWD$(r, \jmath_{\mathrm{T}})$ on line 62 indicates. Crucially, the **fail** invariant on line 60 asserts that the next-hop for a routing packet is *always* defined. The cases for DISPATCHDTC and FORWDDTC in alg. 1 are analogous.

3.3 Ensuring consistent traces

Next-hop routing alone does not guarantee trace consistency, i.e., that the order of events in the trace reflects the one in which these occur locally at SuS processes, def. 1. Trace event reordering arises when a tracer gathers events of a SuS process (we call these *direct events*) and simultaneously receives *routed events* concerning said process from other tracers. Fig. 6a gives another interleaving to the one of fig. 5b to underscore the deleterious effect such a race condition provokes when events are reordered at T_Q. In step 12 T_Q takes over T_P to continue tracing process Q. T_Q collects the event $\star_Q$ in step 15, which happens before T_Q receives the routed event $?_Q$ concerning Q in step 17 of fig. 6a. If T_Q processes events from its trace buffer κ_Q in sequence, as in step 18, it violates trace consistency w.r.t. Q (the correct trace ordering should be "$?_Q.\multimap_Q.\star_Q$"). Naïvely handling $\star$ before $?$ erroneously reflects that Q receives messages after it terminates.

RIARC tracers resolve this issue by prioritising the processing of routed trace events using selective message reception [42]. In doing so, tracers encode the invariant that "*routed* events temporally precede all others that are gathered *directly* by the tracer". RIARC tracers operate in one of two modes, priority (•) and direct (∘), which adequately distinguishes past (i.e., routed) and current (i.e., direct) events from the perspective of the tracer receiving them.

Fig. 6b illustrates this concept. It shows that when in priority mode, T_Q dequeues the routed events $?_Q$ and $\multimap_Q$ labelled by • first. The event $?_Q$ is handled in step 23, whereas $\multimap_Q$ results in the instrumentation of tracer T_R in step 25 of fig. 6b. Meanwhile, T_Q can still receive events directly from Q while priority events are being handled. Yet, direct trace events from Q are considered only *after* T_Q transitions to direct mode. Newly-instrumented tracers default to • mode to implement the described logic; see [8, line 14 in alg. 4 of app. A].



(a) T_Q receives event $\star_Q$ before T_P dispatches $?_Q$. **(b)** T_Q processes events forwarded by T_P first.

Figure 6 Trace event reordering using priority (•) and direct (∘) tracer modes (monitors omitted).

Algorithm 3 Logic handling $\bullet$ trace events, detach request acknowledgements, and forwarding.

```
1  def Loop$_\bullet$($\sigma$,$\varsigma_M$)
2    forever do
3      $r \leftarrow$ next rtd message from trace buffer $\kappa$
4      $m \leftarrow r.m$ # Read embedded message in $r$
5      match $m.\tau$ do
6        case evt : $\sigma \leftarrow$ HandlEvt$_\bullet$($\sigma$,$\varsigma_M$,$r$)
7        case dtc :
           # dtc ack relayed from dispatch tracer
8          $\sigma \leftarrow$ HandlDtc($\sigma$,$\varsigma_M$,$r$)

9  def HandlEvt$_\bullet$($\sigma$,$\varsigma_M$,$r$)
10   $e \leftarrow r.m$
11   match $e.\ell$ do
12     case $\text{-}\diamond$: return HandlSpwn$_\bullet$($\sigma$,$\varsigma_M$,$r$)
13     case $\ast$: return HandlExit$_\bullet$($\sigma$,$\varsigma_M$,$r$)
14     case $!$,$?$: return HandlComm$_\bullet$($\sigma$,$\varsigma_M$,$r$)

15 def HandlSpwn$_\bullet$($\sigma$,$\varsigma_M$,$r$)
16   $e \leftarrow r.m$
17   match $\sigma.\Pi(e.\imath_S)$ do
18     case $\perp$: # No next-hop for $e.\imath_S$; handle $e$
19       AnalyseEvt($\varsigma_M$,$e$)
20       $\imath_T \leftarrow r.\imath_T$ # Read PID of dispatch tracer
21       $\sigma \leftarrow$ Instrument$_\bullet$($\sigma$,$e$,$\imath_T$)
22     case $\jmath_T$: # Next-hop for $e.\imath_S$ exists via $\jmath_T$
23       Forwd($r$,$\jmath_T$)
         # Set next-hop of $e.\jmath_S$ to tracer of $e.\imath_S$
24       $\sigma.\Pi \leftarrow \sigma.\Pi \cup \{\langle e.\jmath_S, \jmath_T\rangle\}$
25   return $\sigma$

26 def HandlExit$_\bullet$($\sigma$,$\varsigma_M$,$r$)
27   $e \leftarrow r.m$
28   match $\sigma.\Pi(e.\imath_S)$ do
29     case $\perp$: # No next-hop for $e.\imath_S$; handle $e$
30       AnalyseEvt($\varsigma_M$,$e$)
31       $\sigma.\Gamma \leftarrow \sigma.\Gamma \setminus \{\langle e.\imath_S, \bullet\rangle\}$
32       TryGC($\sigma$)
33     case $\jmath_T$: Forwd($r$,$\jmath_T$)
34   return $\sigma$

35 def HandlComm$_\bullet$($\sigma$,$\varsigma_M$,$r$)
36   $e \leftarrow r.m$
37   match $\sigma.\Pi(e.\imath_S)$ do
38     case $\perp$: AnalyseEvt($\varsigma_M$,$e$)
39     case $\jmath_T$: Forwd($r$,$\jmath_T$)
40   return $\sigma$

41 def HandlDtc($\sigma$,$\varsigma_M$,$r$)
42   $d \leftarrow r.m$
43   match $\sigma.\Pi(d.\jmath_S)$ do
44     case $\perp$:
45       assert $d.\imath_T =$ self() unexpected dtc ack
46       $\sigma.\Gamma \leftarrow \big(\sigma.\Gamma \setminus \{\langle d.\jmath_S, \bullet\rangle\}\big) \cup \{\langle d.\jmath_S, \circ\rangle\}$
47       if $(\{\langle \imath_S, \gamma\rangle \mid \langle \imath_S, \gamma\rangle \in \sigma.\Gamma, \gamma = \bullet\} = \emptyset)$
48         Loop$_\circ$($\sigma$,$\varsigma_M$) # Put tracer in $\circ$ mode
49     case $\jmath_T$:
50       assert $d.\imath_T \neq$ self() dtc meant for $\imath_T$
51       Forwd($r$,$\jmath_T$)
52   return $\sigma$
```

Loop$_\bullet$ in alg. 3 shows the logic prioritising routed events, which are dequeued on line 3 and handled on line 6. HandlSpwn, HandlExit, and HandlComm in Loop$_\circ$ and Loop$_\bullet$ handle events *differently*. A tracer in direct mode performs *one* of three actions (see alg. 1):

1. it *analyses* events for RV purposes via the function AnalyseEvt(ς_M,e), e.g. line 32,
2. it *dispatches* events that it directly gathers using Dispatch(e,$\jmath_T$), when events ought to be handled by other tracers, e.g. line 33, or
3. it *forwards* routed events to the next-hop through Forwd(r,$\jmath_T$), e.g. line 62.

Tracers in priority mode exclusively handle routed messages as points 1 and 3 describe, e.g. lines 38 and 39 in alg. 3. However, no event dispatching is performed.

3.4 Isolating tracers

A tracer in priority mode coordinates with the dispatch tracer of a particular SuS process it traces. This enables the tracer to determine when *all* of the events of that process have been routed to it by the dispatch tracer. The negotiation is effected using dtc, which the tracer sends to the relevant dispatch tracer. Each tracer records the set of processes it traces in the *traced-processes map*, $\Gamma : \text{Pid}_S \rightharpoonup \{\circ,\bullet\}$. A SuS process mapping is added to Γ when a tracer starts gathering trace events for that process and removed once the process terminates. Lines 6 and 14 in alg. 2 add fresh mappings to Γ; lines 26 in alg. 1 and 31 in alg. 3 purge mappings from Γ. A tracer in priority mode must issue a dtc request *for each* process it tracks in Γ before it can transition to direct mode and start operating on the trace events it gathers directly. The detach request, $d = \langle \mathsf{dtc}, \imath_{\mathrm{T}}, \imath_{\mathrm{S}} \rangle$, contains the PIDs of the issuing tracer and the SuS process to be detached from the dispatch tracer. Once the tracer receives an acknowledgement to the dtc request for the SuS PID $d.\imath_{\mathrm{S}}$ from the dispatch tracer, it updates the corresponding entry $d.\imath_{\mathrm{S}} \mapsto \bullet$ in Γ, marking it as detached, $d.\imath_{\mathrm{S}} \mapsto \circ$. Alg. 3 shows this logic on line 46. A tracer transitions from priority to direct mode once *all* the processes in its Γ map are marked detached; line 47 in alg. 3 performs this check. Once in direct mode, tracers are isolated from others in the choreography.

Fig. 6b depicts the tracer T_Q in priority mode sending the detach request $\langle \mathsf{dtc}, q_{\mathrm{T}}, q_{\mathrm{S}} \rangle$ for SuS PID q_{S} to the dispatch tracer. This happens in step ⑬, after T_Q starts tracing Q directly in step ⑫. Alg. 2 effects this transaction with the dispatch tracer by the operation Detach on line 13; see [8, app. A] for definition of Detach. The dtc request issued by T_Q is deposited in the trace buffer of the dispatch tracer T_P after the events $?_Q$ and $\text{-}\!\!\diamond_Q$. T_P processes the messages in its buffer sequentially in ⑩, ⑰, ⑲, ⑳ and ㉘, and forwards $?_Q$ and $\text{-}\!\!\diamond_Q$ to T_Q, steps ⑱ and ㉑. Crucially, T_P *acknowledges* the dtc request issued by T_Q: T_P dispatches dtc back to tracer T_Q, as step ㉙ indicates. T_Q first handles the events $?_Q$ and $\text{-}\!\!\diamond_Q$ (tagged with $\bullet$ in fig. 6b) in steps ㉓ and ㉔. Lastly, T_Q handles dtc in ㉚ and marks process Q as detached from its dispatch tracer T_P. The update on the traced-process map Γ is performed by HandlDtc on line 46 in alg. 3. Tracer T_Q in fig. 6b transitions to direct mode in step ㉛, when the only process Q that it traces is detached. T_Q resumes handling $\star_Q$ in step ㉜, which is consistent w.r.t. the events exhibited locally at Q, i.e., "$?_Q.\text{-}\!\!\diamond_Q.\star_Q$".

An acknowledgement to a detach request sent from a dispatch tracer, $\langle \mathsf{dtc}, \imath_{\mathrm{T}}, \imath_{\mathrm{S}} \rangle$, is generally propagated through multiple next-hops before it reaches the tracer with PID $\imath_{\mathrm{T}}$ issuing the request. Since a dtc request informs the dispatch tracer that $\imath_{\mathrm{T}}$ is gathering trace events for the SuS PID $\imath_{\mathrm{S}}$ *directly*, the next-hop entries in the routing maps of tracers on the DAG path from the dispatch tracer to $\imath_{\mathrm{T}}$ are *stale*. Each tracer on this DAG path purges the next-hop entry for the SuS PID $\imath_{\mathrm{S}}$ in Γ once it forwards dtc to the neighbouring tracer. DispatchDtc and ForwdDtc in alg. 1 perform this clean-up. Fig. 6b does not illustrate the latter clean-up flow, which we summarise next. After receiving dtc, the dispatch tracer T_P removes from Π_P the next-hop mapping $q_{\mathrm{S}} \mapsto q_{\mathrm{T}}$ and calls DispatchDtc to acknowledge the detach request $\langle \mathsf{dtc}, q_{\mathrm{T}}, q_{\mathrm{S}} \rangle$ it receives from T_Q. Similarly, T_P removes $r_{\mathrm{S}} \mapsto q_{\mathrm{T}}$ once it acknowledges the detach request $\langle \mathsf{dtc}, r_{\mathrm{T}}, r_{\mathrm{S}} \rangle$ sent from T_R. Once T_Q receives the routing packet $\langle \mathsf{rtd}, p_{\mathrm{T}}, \langle \mathsf{dtc}, r_{\mathrm{T}}, r_{\mathrm{S}} \rangle \rangle$ that embeds the detach acknowledgement T_P sends, it removes the next-hop mapping $r_{\mathrm{S}} \mapsto r_{\mathrm{T}}$ from Π_Q. T_Q then forwards this dtc acknowledgement to T_R.

RIARC ensures that all routing packets carrying dtc acknowledgements terminate at the tracers that issued these dtc requests. This requires *one* of two tracer conditions to hold:

1. either the tracer cannot forward the dtc acknowledgement to a next-hop, meaning that the tracer sent the dtc request, or
2. the tracer can forward the dtc acknowledgement via a next-hop, in which case the tracer did not issue the dtc request.

Alg. 3 enforces this invariant on lines 44 and 45 for case 1, and on lines 49 and 50 for case 2.

3.5 Minimising overhead

Instrumenting specific processes – in contrast to fully instrumenting the SuS – reduces the volume of gathered trace events and helps lower the runtime overhead induced. RIARC uses the instrumentation map, $\Lambda : \textsc{Sig}_{\mathrm{S}} \rightharpoonup \textsc{Sig}_{\mathrm{M}}$, to this end. Λ specifies the SuS function signatures to instrument and the corresponding RV monitor signatures tasked with the analysis via AnalyseEvt. RIARC utilises the signature $e.\varsigma_{\mathrm{S}}$ carried by spawn events $e = \langle \mathsf{evt}, \text{-}\!\!\diamond, \imath_{\mathrm{S}}, \jmath_{\mathrm{S}}, \varsigma_{\mathrm{S}} \rangle$ to determine whether the SuS process spawning $e.\varsigma_{\text{S}}$ requires a separate tracer. The Instrument operations in alg. 2 perform this check against Λ (lines 2 and 9). If a separate tracer is not required, $e.\jmath_{\text{S}}$ is instrumented using the tracer of its parent process, $e.\imath_{\text{S}}$; see tracing assumptions A_1 and A_2. This logic caters for all the set-ups shown in figs. 1b, 1c, and 2b.

3.6 Shrinking the set-up

RIARC remains elastic by discarding unneeded tracers. Tracers in direct and priority mode purge SuS PID references from the traced-process map when handling $\ast$ trace events. HandleExit$_\circ$ and HandleExit$_\bullet$ implement this logic in algs. 1 and 3 on lines 26 and 31. Tracer termination does *not* occur when the tracer has no processes left to trace, i.e., when $\Gamma = \emptyset$, since the tracer may be required to forward trace events to neighbouring tracers. Instead, tracers perform a garbage collection check each time a mapping from Γ or Π is removed. A tracer terminates when $\Gamma = \Pi = \emptyset$, indicating that it has no SuS processes left to trace or any next-hop forwarding to perform. TryGC used on lines 27, 41, and 55 in alg. 1, as well as on line 32 in alg. 3 encapsulates this check. Note that garbage collection never prematurely disrupts the RV analysis that tracers conduct, as invocations to AnalyseEvt always precede TryGC checks in our logic of algs. 1 and 3.

4 Correctness validation

We assess the validity of RIARC in two stages. First, we confirm its implementability by instantiating the core logic of algs. 1−3 to Erlang. Our implementation targets two RV scenarios: online and offline monitoring [64, 22]. Second, we subject the implementation to a series of systematic tests using a selection of instrumentation set-ups. These tests exhaustively emulate the interleaved execution of the SuS and tracer processes by generating all the *valid* permutations of events in a set of traces. This exercises the tracer choreography invariants mentioned in sec. 3, confirming the integrity of the tracer DAG topology under each interleaving. We also use specialised RV monitor signatures in AnalyseEvt to assert the soundness (def. 1) of trace event sequences analysed by tracers; see algs. 1 and 3 in sec. 3.

4.1 Implementability

Our implementation of RIARC maps the tracer processes from sec. 3 to Erlang actors.The routing (Π), instrumentation (Λ), and traced-processes (Γ) maps constituting the tracer state σ are realised as Erlang maps for efficient access. Trace event buffers κ coincide with actor mailboxes, while the remaining logic in algs. 1−3 translates directly to Erlang code. This one-to-one mapping gives us confidence that our implementation reflects the algorithm logic.

In *online* RV, monitors analyse trace events while the SuS executes, whereas the *offline* setting defers this analysis until the system terminates; [8, fig. 11 in app. B.1] captures the distinction in process tracing between online and offline instrumentation in our setting (showing trace buffers only). The online instrumentation set-up employs the tracing infrastructure offered by the EVM, which deposits SuS trace event messages in tracer mailboxes. Erlang tracing complies with tracing assumption A_1, enabling RIARC to instrument disjoint SuS processes sets. We configure the EVM with the `set_on_spawn` flag so that spawned processes automatically inherit the same tracer as their parent [42]. This tracer assignment is atomic, meeting tracing assumption A_2. We also use the `procs`, `send`, and `receive` tracing flags, which constrain the events emitted by the EVM to $-\!\diamond$, $\ast$, $!$, and $\ast$. The EVM enforces single-process tracing, i.e., tracing assumption A_3, and guarantees that $-\!\diamond$ events of descendant processes are causally-ordered [128], i.e., tracing assumption A_4.

The offline counterpart differs only in its tracing layer, where events are read as *recorded* runs of the SuS. Recorded runs can be acquired externally, e.g. using DTrace [36] or LTTng [56], making it possible to monitor systems that execute outside of the EVM. Our bespoke offline tracing engine of [8, fig. 11b in app. B.1] fulfils tracing assumptions $A_1 - A_4$. This is crucial since it permits the *same* implementation of RIARC to be used in online and offline settings. Sec. 4.2 leverages this aspect to validate RIARC exhaustively using trace permutations.

We develop two versions of the TRACE, CLEAR, and PREEMPT functions of [8, alg. 5 in app. A] to standardise tracing for online and offline use. The overloads for online use access the EVM tracing via the Erlang built-in primitive `trace` [42]. The second set of overloads wraps around our offline tracing engine to replay files containing specifically-formatted trace events. Offline tracing relaxes tracing assumption A_4, as recorded runs do not generally guarantee that the -◇ events of descendant SuS processes are causally ordered. Our offline tracing logic relies on the PID information carried by -◇ events to rearrange them and recover the causal ordering per tracing assumption A_4. TRACE($\imath_S$,$\imath_T$) registers a tracer $\imath_T$ with the offline tracing engine, which maintains an event buffer for $\imath_T$, together with a set of SuS PIDs that $\imath_T$ traces. A tracer can use TRACE with multiple SuS PIDs to register to obtain events for a process set, i.e., tracing assumption A_1. The tracing engine accumulates the events it reads from file in each tracer buffer and delivers events to the corresponding tracer mailbox once the casual ordering between -◇ events of descendant SuS processes is established. Our offline tracing engine implements tracing inheritance (tracing assumption A_2) and enforces single-process tracing (tracing assumption A_3); [8, ex. 7 in app. B.1] sketches how the tracing engine uses its internal tracer buffers to deliver events to tracers.

4.2 Correctness

Conventional testing does not guarantee the absence of concurrency errors due to the different interleaved executions that may be possible [105]. While subjecting the system under test to high loads raises the likelyhood of obtaining more coverage, this still depends on external factors, such as scheduling, which dictate the executions induced in practice. Controlling the conditions for concurrency testing requires a *systematic exploration* of all the interleaved executions [74]. In fact, it is *not the size* of the testing load that matters, but the choice of interleaved executions that exhaust the space of possible system states [14]. Concuerror [48] is a tool for systematic Erlang code testing. Unfortunately, we could not use Concuerror to test our RIARC implementation, as we were unable to integrate it with Erlang tracing.

We, nevertheless, adopt the systematic scheme advocated by Concuerror. Our approach uses the offline tracing tool described in sec. 4.1 to induce specific interleaved sequences for instrumentation set-ups, such as those of figs. 1b, 1c, and 2a. We obtain these sequences by taking all the sound (def. 1) event permutations of traces produced by the SuS. These sequences are then replayed by the offline tracing engine to systematically induce interleaved SuS executions. Our final RIARC implementation embeds further invariants besides those mentioned in sec. 3, e.g. the **assert** and **fail** statements in algs. 1 and 3. Readers are referred to [8, app. B.2] for the full list. We ascertain *trace soundness* for each SuS interleaving that is emulated. This is accomplished via the function ANALYSEEVT, which we preload with monitors that assert the event sequence expected at each tracer. We also use identical tests in our empirical evaluation of sec. 5 under high loads. It is worth mentioning that while we systematically drive the execution of the SuS, we do not control the execution of tracers. Yet, we indirectly induce various dynamic tracer arrangements in the monitor DAG topology under the different groupings of SuS process sets that tracers instrument. For example, we fully instrument system depicted in fig. 2a in all its configurations, e.g. $\mathcal{C}_1 = [T_{\{P\}} \rightsquigarrow$

$\{P\},T_{\{Q\}} \rightsquigarrow \{Q\},T_{\{R\}} \rightsquigarrow \{R\}]$, $\mathcal{C}_2 = [T_{\{P,Q\}} \rightsquigarrow \{P,Q\},T_{\{R\}} \rightsquigarrow \{R\}]$, ..., $\mathcal{C}_5 = [T_{\{P,Q,R\}} \rightsquigarrow \{P,Q,R\}]$, as well as instrument it partially, e.g. $\mathcal{C}_6 = [T_{\{P\}} \rightsquigarrow \{P\}]$, $\mathcal{C}_7 = [T_{\{P,Q\}} \rightsquigarrow \{P,Q\}]$, etc. Each of these configurations, when individually paired with every fabricated interleaved execution of the SuS, indicate that our RIARC implementation and corresponding logic of sec. 3 is correct.

5 Empirical evaluation

We assess the feasibility of our RIARC implementation, confirming it safeguards the *responsive*, *resilient*, *message-driven*, and *elastic* attributes of the SuS. Sec. 4 targets a small selection of instrumentation set-ups to induce interleaved execution sequences and validate correctness exhaustively. We now employ *stress testing* [109] to investigate how RIARC performs in terms of the *runtime overhead* it exhibits. Our study focusses on *online* monitoring, as its overhead requirement is far more stringent than offline monitoring [63, 64, 22, 71]. We evaluate RIARC against inline instrumentation since the latter is regarded as the most efficient instrumentation technique [62, 61, 22]. This comparison establishes a solid basis for our results to be generalised reliably. We also compare RIARC to centralised instrumentation to confirm that the latter approach does not scale under typical loads.

Our experiments are extensive. We use two hardware platforms to model edge-case scenarios based on limited hardware and general-case scenarios using commodity hardware. The evaluation subjects inline, centralised, and RIARC instrumentation to high loads that go beyond the state of the art and use realistic workload profiles. We gauge overhead under three performance metrics, the *response time*, *memory consumption*, and *scheduler utilisation*, which are crucial for reactive systems [7, 109]. Our results confirm that the overhead RIARC induces is adequate for applications such as soft real-time systems [42, 94], where the latency requirement is typically in the order of seconds [92]. We also show that RIARC yields overhead comparable to inlining in settings exhibiting moderate concurrency.

5.1 Benchmarking tool

Benchmarking is standard practice for gauging runtime overhead in software [100, 77, 35]. Frameworks, including DaCapo [28] and Savina [84], offer limited concurrency, making them inapplicable to our case; see [8, app. C.1] for detailed reasons. Industry-proven *synthetic* load testing benchmarking tools cater to reactive systems, e.g. Apache JMeter [67], Tsung [115], and Basho Bench [23]. Their general-purpose design, however, necessarily treats systems as a black box by gathering metrics externally, which may impact measurement *precision* [7]. Moreover, these load testers generate standard workloads, e.g. Poisson processes [79, 102, 89], but lack others, e.g. load bursts, that replicate typical operation or induce edge-case stress.

We adopt BenchCRV [7], another synthetic load testing tool specific to RV benchmarking for reactive systems. BenchCRV sets itself apart from the tools mentioned above because it does not require external software (e.g., a web server) to drive tests. Instead, BenchCRV produces different SuS models that *closely emulate* real-world software behaviour. These models are based on the master-worker paradigm [120]: a pervasive architecture in distributed (e.g. Big Data stream processing frameworks, render farms) and concurrent systems [129, 73, 55, 132]. Like Tsung and Basho Bench, BenchCRV exploits the lightweight EVM process model to generate highly-concurrent synthetic workloads.

BenchCRV creates master-worker models and induces workloads derived from configurable parameters. In these models, the master process spawns a series of workers and allocates tasks. The volume of workers per benchmark run is set via the parameter n. Each worker task consists of a *batch* of requests that the worker receives, processes, and echoes back to the master process. The amount of requests batched in one task is given by the parameter w. Workers terminate when all of their allotted tasks are processed and acknowledged by the master. BenchCRV creates workers based on *workload profiles.* A profile dictates how the master spreads its creation of workers along the loading timeline, t, given in seconds. BenchCRV supports three workload profiles based on ones typical in practice:

Steady models the SuS under stable workload (Poisson process).

Pulse models the SuS under gradually rising and falling workload (Normal distribution).

Burst models the SuS under stress due to workload spikes (Log-normal distribution).

BenchCRV records three performance metrics to give a multi-faceted view of system overhead:

Mean response time in milliseconds (ms), gauging monitoring latency effects on the SuS.

Mean memory consumption in GB, gauging monitoring memory pressure on the SuS.

Mean scheduler utilisation as a percentage of the total processing capacity, showing how monitors maximise the scheduler use.

The prevalent use of the master-worker paradigm, the veracity with which BenchCRV models systems, the range of realistic workload profiles, and the choice of runtime metrics it gathers make this tool ideal for our experiments. We refer readers to [8, app. C.2] and [7] for details.

5.2 Benchmark configuration

The BenchCRV master-worker models we generate take the role of the SuS in our experiments. We consider *edge-case* and *general-case* hardware platform set-ups for the following reasons:

$\mathsf{P_E}$ **Edge-case** captures platforms with *limited* hardware. It uses an Intel Core i7 M620 64-bit CPU with 8GB of memory, running Ubuntu 18.04 LTS and Erlang/OTP 22.2.1.

$\mathsf{P_G}$ **General-case** captures platforms with *commodity* hardware. It uses an Intel Core i9 9880H 64-bit CPU with 16GB of memory, running macOS 12.3.1 and Erlang/OTP 25.0.3.

The EVMs on platforms $\mathrm{P_E}$ and $\mathrm{P_G}$ are set with 4 and 16 scheduling threads, respectively. These scheduler settings coincide with the processors available on each SMP [12] platform. We also use the $\mathrm{P_E}$ and $\mathrm{P_G}$ platforms with two concurrency scenarios for reactive systems:

$\mathsf{C_H}$ **High concurrency scenarios** perform short-lived tasks, e.g. web apps that fulfil thousands of HTTP client requests by fetching static content or executing back-end commands.

$\mathsf{C_M}$ **Moderate concurrency scenarios** engage in long-running, computationally-intensive tasks, e.g. Big Data stream processing frameworks.

Our benchmark workloads match the hardware capacity afforded by $\mathrm{P_E}$ and $\mathrm{P_G}$:

High concurrency benchmarks on $\mathrm{P_E}$ set $n = 100\text{k}$ workers and $w = 100$ work requests per worker. These generate $\approx (n \times w \text{ requests} \times w \text{ responses}) = 20\text{M}$ message exchanges between the master and worker processes, totalling $\approx (20\text{M} \times ! \text{ events} \times ? \text{ events}) = 40\text{M}$ analysable trace events. Platform $\mathrm{P_G}$ sets $n = 500\text{k}$ workers batched with $w = 100$ requests to produce $\approx 100\text{M}$ messages and $\approx 200\text{M}$ trace events. The high concurrency model $\mathrm{C_H}$ is studied in sec. 5.4.

Moderate concurrency benchmarks on $\mathrm{P_G}$ set $n = 5\text{k}$ workers and $w = 10\text{k}$ work requests per worker. These settings yield roughly the same number of trace events as on $\mathrm{P_G}$ with concurrency scenario $\mathrm{C_H}$. The moderate concurrency model $\mathrm{C_M}$ is studied in sec. 5.5.

All experiments in secs. 5.4 and 5.5 use a total loading time of $t = 100\text{s}$. Each experiment consists of *ten* benchmarks that apply Steady, Pulse, and Burst workloads. We repeat every experiment *thrice* to obtain *negligible variability* and ensure the accuracy of our results; see [8, app. C.4] for a summary of these workloads and [8, app. C.5] for the precautions we take.

The hardware, OS, and Erlang versions of platforms $\mathrm{P_E}$ and $\mathrm{P_G}$, combined with the workloads of concurrency scenarios $\mathrm{C_H}$ and $\mathrm{C_M}$ provide generality to our conclusions.

5.3 Instrumentation configuration

One challenge in conducting our experiments is the lack of RV monitoring tools targeting the EVM. To the best of our knowledge [64, tables 3 and 4], detectEr [72, 18, 19, 17, 70, 40] is the only RV tool for Erlang that implements centralised outline instrumentation[2]. We are unaware of inline RV tools besides [38] and [3, 4]. Since the former tool is *unavailable*, we use the latter, more recent work[3]. In our experiments, we instrument the master *and each* worker process in the SuS models generated from sec. 5.2 to exert the highest possible load and capture *worst-case* scenarios. BenchCRV annotates work requests and responses with a unique sequence number to account for each message in benchmark runs. We leverage this numbering to write specialised monitor replicas that ascertain the *soundness* of trace event sequences reported to every RV monitor linked with the master and workers; see [8, app. C.5] for details. Equally crucial, this runtime checking introduces a degree of *realistic* RV analysis slowdown that is *uniform* across all monitors in the inline, centralised, and RIARC monitoring set-ups. We empirically estimate this slowdown at ≈ 5µs per analysed event.

5.4 High concurrency benchmarks

We study runtime overhead in the high concurrency scenario C_H with two aims. First, we show the effect overhead has on the SuS as it executes. Specifically, we consider how the memory consumption and scheduler utilisation impact the *latency* a client of the SuS experiences, e.g. end-user or application. We use the edge-case platform P_E for these experiments; analogous results obtained on P_G are detailed in [8, app. C]. Our second goal targets the general-case platform P_G to assess the *scalability* of the instrumentation methods through their optimal use of the *additional* memory and scheduler capacity afforded by P_G.

The charts in secs. 5.4.1 − 5.4.3 plot performance metrics, e.g. memory consumption (y-axis) against the number of concurrent worker processes or the execution duration (x-axis). Since inline instrumentation prevents us from delineating the SuS and monitoring-induced runtime overhead, we follow the standard RV literature practice and include the *baseline* plots, e.g. [19, 72, 46, 38, 99, 114, 112]. Baseline plots show the *unmonitored* SuS to compare the relative overhead between each evaluated instrumentation method.

5.4.1 Instrumentation overhead

The first set of experiments isolates the instrumentation overhead induced on the SuS: this is the aggregated cost of tracing *and* reporting the traces soundly per def. 1 to RV monitors. Crucially, these experiments *omit monitors*, as we want to quantify the instrumentation overhead and understand its impact on the SuS. This enables us to focus on the differences between inlining – regarded as the most efficient instrumentation method [62, 61, 22] – and outlining. As far as we know [64, 71], outlining has *never* been used for decentralised RV in a *dynamic* setting such as ours. While we confirm that inline instrumentation uses less memory and scheduler capacity, RIARC dynamically scales and economises their use *without* adverse impact on the latency. In fact, the latency induced by RIARC is a mere 519ms higher than that of inline instrumentation at the peak stress-inducing loading point of 3.7k workers/s under Burst workloads. Our experiments indicate that centralised instrumentation manages resources poorly due to its inability to scale, increasing the chances of failure; see sec. 5.4.2.

[2] `https://bitbucket.org/duncanatt/detecter-lite`
[3] `https://github.com/ScienceofComputerProgramming/SCICO-D-22-00294`

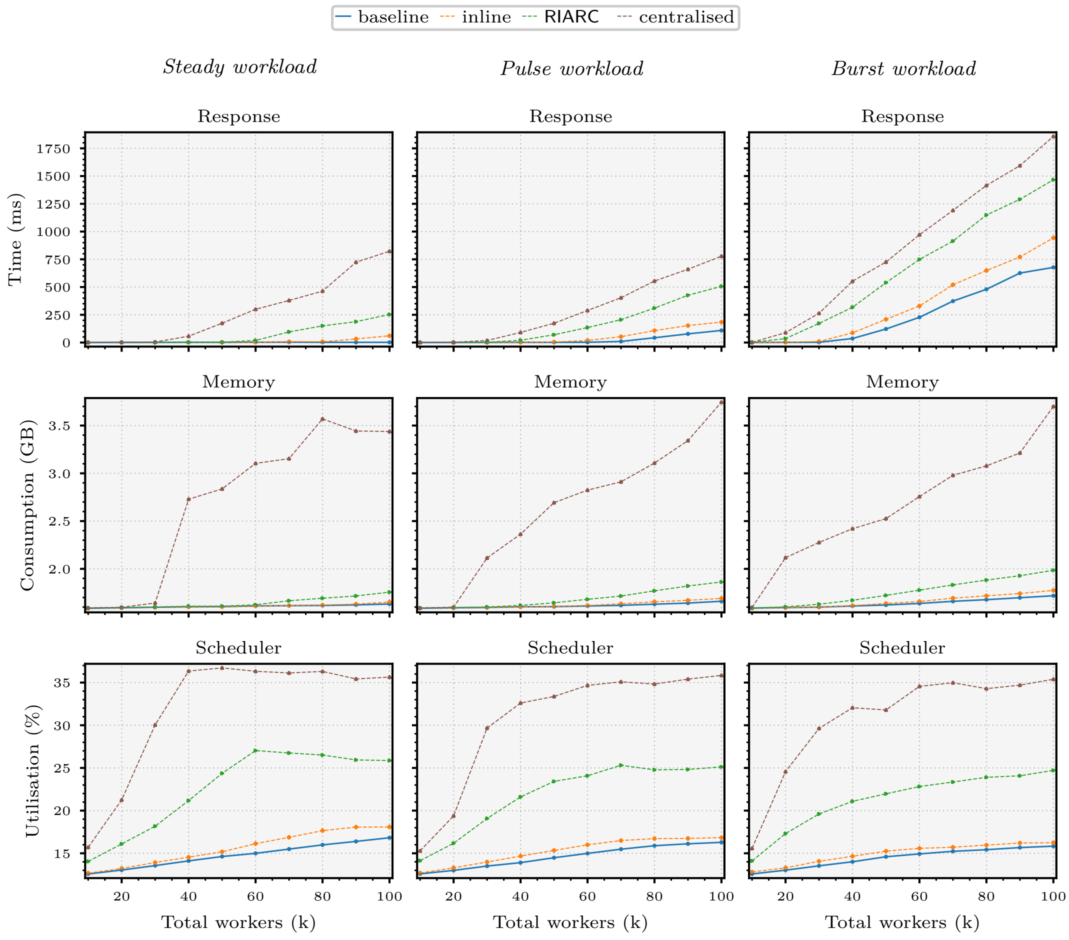


Figure 7 Isolated instrumentation overhead (*high* workload, 100k workers).

Fig. 7 plots our results. Centralised instrumentation carries the largest overhead penalty. Regardless of the workload applied, it uses the most memory, ≈ 3.8GB, highlighting its ineptitude to scale. This stems from the backlog of trace event messages that accumulate in the mailbox of the central tracer and is a manifestation of two aspects. First, the central tracer does not consume events at the same rate worker processes produce them. Evidence of this *bottleneck* is visible as high scheduler utilisation in fig. 7 (bottom). This values settles at $\approx 36\%$ for the benchmarks with ≈ 40k workers under the Steady workload and ≈ 60k workers under Pulse and Burst workloads. Interpreting these $< 36\%$ scheduler usage values in isolation may suggest that centralised instrumentation has the potential to scale. However, its memory consumption plots in fig. 7 (middle) contradict this erroneous hypothesis.

By contrast, RIARC uses fewer resources to yield lower response times across the three workloads. The scheduler utilisation for RIARC slightly plateaus in the Steady ($\approx$60k workers) and Pulse (≈ 70k workers) workload charts. This is not owed to scalability limitations of RIARC but to the intrinsic throttling instigated by the master process [120]. In fact, the plots for the baseline system and inline instrumentation in fig. 7 (middle) exhibit analogous signs of throttling. Even at a peak Burst workload of 3.7k workers/s, inline and RIARC instrumentation consume fairly similar amounts of memory, 1.7GB vs. 1.9GB, respectively.

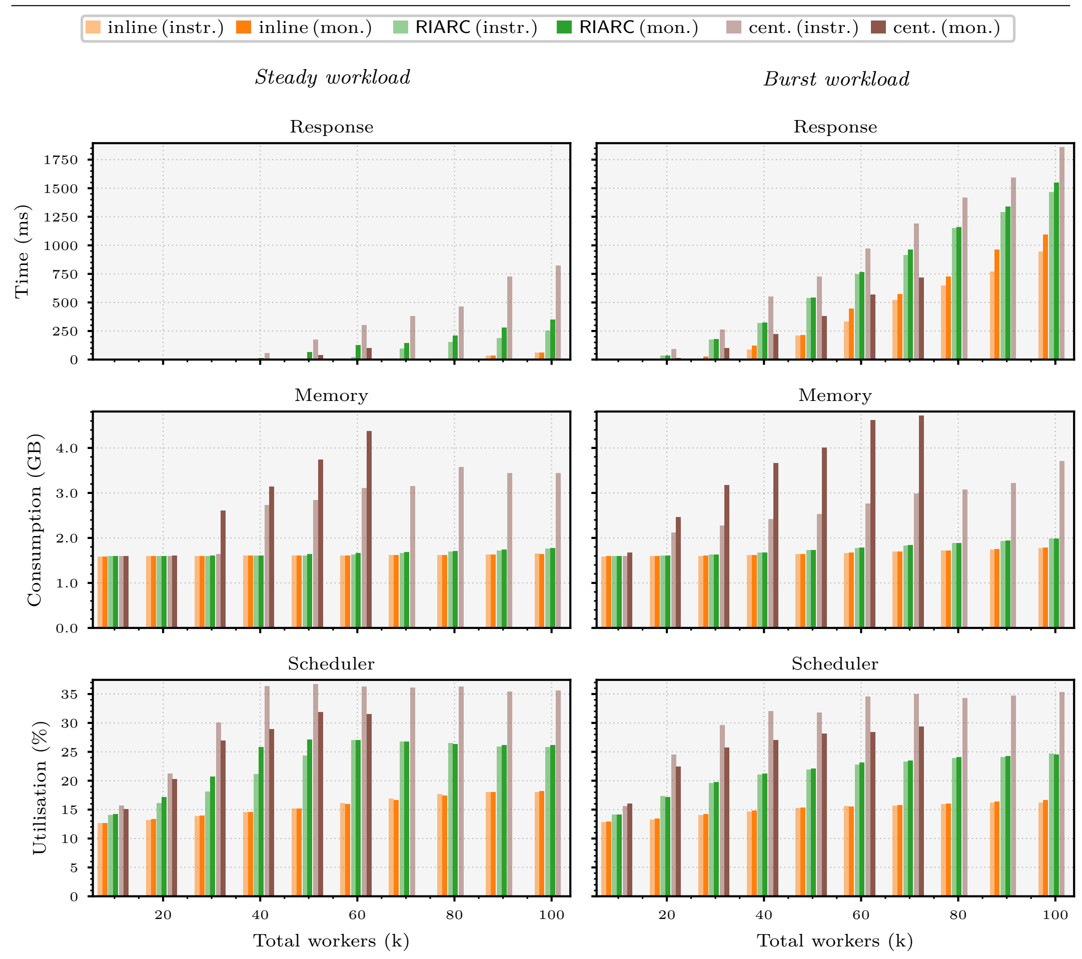


Figure 8 Instrumentation and RV monitoring overhead gap (*high* workload, 100k workers).

5.4.2 Monitoring overhead

Our second set of experiments extends the results of sec. 5.4.1 and quantifies the cost of RV monitoring. The *runtime monitoring* overhead combines the instrumentation and slowdown due to the RV analysis, established at ≈ 5µs per event in sec. 5.3 for our experiments. Fig. 8 plots the instrumentation (*instr.*) overhead from sec. 5.4.1 next to the runtime monitoring overhead (*mon.*). It shows that the RV analysis slowdown aggravates centralised monitoring to the point of crashing. Inline and RIARC monitoring are minimally affected. Our results also reveal that the instrumentation incurs the *major* overhead portion, not the RV analysis. Sec. 5.6 comments on this finding in the context of existing RV tools.

Fig. 8 plots our results under the Steady and Burst workloads; [8, fig. 14 in app. C.6.1] includes all three workloads. The charts for centralised monitoring exhibit a significant disparity between the instrumentation and runtime monitoring bar plots as the workload increases. This trend is consistent across both workloads in fig. 8. The lack of scalability of centralised monitoring in fig. 8 manifests as an increase in memory consumption but stabilised scheduler usage, as in fig. 7. Memory consumption and scheduler usage for centralised monitoring grow rapidly beyond ≈ 30k and ≈ 20k workers under the Steady and Burst workloads, respectively. Bottlenecks led our experiments to crash (shown as missing bar plots in fig. 8). Crashes occur at ≈ 70k workers under the Steady and at ≈ 80k under Burst workload. By analysing the resulting dumps, we could attribute these crashes to memory exhaustion, which caused the EVM to fail. The dumps indicate severe memory pressure due to the vast backlog of trace event messages in the mailbox of the central tracer.

Inline and RIARC monitoring scale to accommodate the RV analysis slowdown. This is confirmed by cross-referencing the memory consumption and scheduler utilisation in fig. 8 for both monitoring methods. Each displays comparable overhead in their respective instrumentation and corresponding runtime monitoring bar plots. Fig. 8 (top) shows that inline and RIARC monitoring increase the latency, albeit for different reasons. The internal operation of RIARC enables us to deduce that its latency stems from message routing and dynamic tracer reconfiguration. Its scheduler utilisation plots support this observation. The latency due to inlining is a direct effect of RV analysis slowdown, provoked by the lock-step execution of monitors and the SuS. Other works, e.g. [46, 37], offer similar observations.

Dissecting our results uncovers further subtleties. The optimal scheduler utilisation of RIARC implies that its monitors are only active when triggered by trace events but remain idle otherwise. This inference is supported by the absence of sudden or continued memory growth for RIARC in fig. 8 (middle). The instrumentation and runtime monitoring latency bar plots for inline monitoring exhibit a growing pairwise gap that starts at ≈ 80k workers in fig. 8 (top right). The respective gap for RIARC at this mark is perceptibly lower. We credit this lower latency gap to outlining, which absorbs the slowdown effect of RV analyses. This leads us to conjecture that RIARC could accommodate monitors that perform richer RV analyses with minimal impact on the SuS. Our calculations from fig. 8 (top right) put the latency at 1093ms for inline monitoring vs. 1547ms for RIARC at a peak Burst workload of 3.7k workers/s: a 454ms difference, which is *lower* than the 519ms gap measured in sec. 5.4.1. Sec. 5.5 shows this gap is negligible in moderate concurrency scenarios.

5.4.3 Resource usage

We employ platform $\mathrm{P_G}$ with high concurrency $\mathrm{C_H}$ to confirm that our observations about inline and RIARC monitoring transfer to general cases. Secs. 5.4.1 and 5.4.2 deem centralised monitoring to be impractical. We, thus, omit it from the sequel; see [8, app. C.6.3] for results.

Our experiments now use 16 scheduling threads, $n = 500$k workers, and $w = 100$ requests per worker, producing ≈ 100M messages and ≈ 200M trace events; [8, fig. 13 in app. C.4] render these Steady, Pulse, and Burst workload models. Secs. 5.4.1 and 5.4.2 bound the memory and scheduler metrics to the period the SuS executes to portray the *actual overhead* impact on the system. We refocus that view to assess the monitoring overhead in *its entirety* – from the point of SuS launch until monitors complete their RV analysis. Doing so reveals how inline and RIARC monitoring optimise the use of added memory and processing capacity. Results show that inline and RIARC monitoring are elastic and dynamically adapt to changes in the applied workloads; [8, app. C.6.3] confirms that centralised monitoring lacks this trait.

Fig. 9 gives a complete benchmark run under the Steady and Burst workloads. We relabel the x-axis with the benchmark duration and omit the response time plots since response time is inapplicable to these experiments (latency is an attribute of the SuS, not the monitors). In this run, the Steady workload generates a sustained load of ≈ 5k workers/s whereas Burst peaks at ≈ 17.8k workers/s under maximum load at ≈ 5s; see [8, fig. 13 in app. C.4].

Fig. 9 (top) illustrates the memory consumption patterns for inline and RIARC monitoring, which exhibit *elasticity*. This elastic behaviour occurs at different points in the plots. Inline monitoring peaks at ≈ 3.7GB at ≈ 72s and RIARC at ≈ 5.7GB at ≈ 100s under the Burst workload. The memory consumption for both methods stabilises at around ≈ 36s under the Steady workload, with ≈ 2.3GB for inline and ≈ 2.7GB for RIARC monitoring.

Elasticity in these methods is due to different reasons: it is intrinsic to inline monitoring (see sec. 1), whereas the RIARC spawns and garbage collects monitors on demand (secs. 3.1 and 3.6). These observations are certified by [8, fig. 16 in app. C.6.3] under the Pulse workload. Centralised monitoring is *insensitive* to the workload applied, as [8, figs. 17 and 18 in app. C.6.3] reconfirm.

The effect of dynamic message routing and tracer reconfiguration that RIARC performs is evident in the scheduler utilisation plots of fig. 9. Under the Steady and Burst workloads, scheduler utilisation oscillates continually due to the sustained influx of trace events. Oscillations corroborate our observation in sec. 5.4.2 about RIARC, namely, that monitors are activated by trace events but remain idle otherwise. Active monitor periods manifest as peaks in fig. 9. Idle periods, where monitors are placed in the EVM waiting queues, are reflected as regions with low and stable scheduler utilisation. These oscillations showcase the message-driven aspect of RIARC, which analyses events asynchronously. Inlining exhibits minimal scheduler utilisation oscillations due to its lock-step execution with the SuS.

5.5 Moderate concurrency benchmarks

Our last experiment studies moderate concurrency scenarios C_M. The general-case platform P_G sets $n = 5$k workers and $w = 10$k requests per worker, and uses 16 EVM schedulers. We show that under these loads, RIARC induces overhead on par with inline monitoring.

Moderate concurrency alters the execution of the master-worker model, compared to our benchmarks of secs. 5.4.1 – 5.4.3. In this set-up, the master creates most of its worker processes at the initial stage of benchmark runs and spends the remaining time allocating work requests. This change grows the request throughput, e.g. see [8, tbl. 5 in app. C.4]. One consequence is that centralised monitoring consistently crashes under the rapid accumulation of messages in its mailbox. We, thus, limit our study to inline and RIARC monitoring.

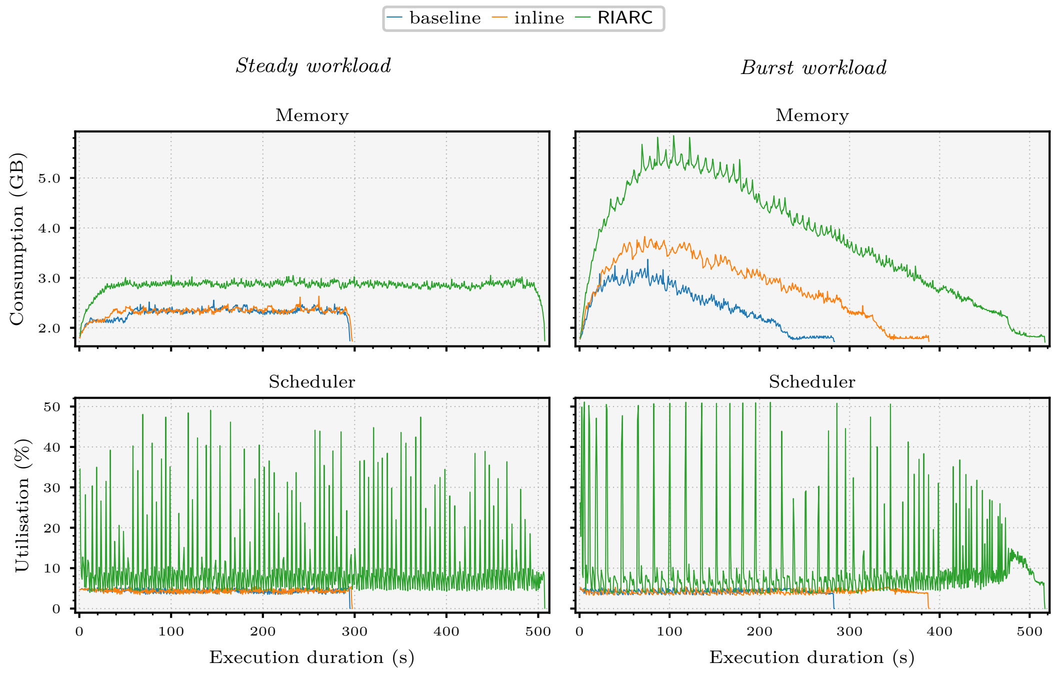


Figure 9 Inline and RIARC monitoring resource usage (*high* workload, 500k workers).

Tbl. 3 compares the results taken on platform P_G from sec. 5.4.3 with 500k workers (high concurrency, C_H) against the ones on P_G with 5k workers (moderate concurrency, C_M). The figures shown estimate the percentage overhead w.r.t. the baseline systems C_H and C_M at this *maximum* load. Our ensuing discussion is limited to the overhead under the Steady and Burst workloads since each respectively captures the SuS operation in *typical* and *severe* load conditions. Readers are referred to [8, fig. 20 in app. C.6.4] for the overhead comparison given in absolute metric values for the entirety of benchmark runs.

Tbl. 3 indicates that the memory consumption overhead due to inline monitoring is not affected under the Steady workload, which remains at 1% in both the high and moderate concurrency scenarios C_H and C_M. However, it decreases from 16% in C_H to 1% in C_M. We observe the opposite effect on the scheduler utilisation overhead for inline monitoring. For the moderate concurrency case C_M, the scheduler overhead under the Steady and Burst workloads increases to 3% and 4% respectively.

Tbl. 3 also shows that under the Steady workload, RIARC induces a 23% memory overhead in concurrency scenario C_H vs. 8% in concurrency scenario C_M, a decrease of 15%. Under the Burst workload, this overhead is reduced by 46%, from 56% in C_H to 10% in C_M. The scheduler utilisation overhead for RIARC from C_H to C_M also registers drops of $\approx$71% under both Steady and Burst workloads. We attribute these overhead improvements to the lower number of worker processes the master creates in the moderate concurrency set-up, C_M. The long-running worker processes induce stability in the SuS. RIARC adapts to this change favourably by performing fewer trace event routing and tracer reconfigurations. The ramification of this adaptability is perceivable in the latency overhead discussed next.

RIARC inflates the latency overhead from 95% in C_H to 194% in C_M under the Steady workload (+99%), and from 97% in C_H to 190% in C_M under the Burst workload (+93%). However, RIARC induces *less latency* overhead than inline monitoring. Tbl. 3 reveals that the latency overhead for inline monitoring grows from 4% in the high concurrency set-up C_H to 246% in the moderate concurrency set-up C_M under the Steady workload (+242%). It also grows under the Burst workload, from 55% in C_H to 193% in C_M (+138%). In fact, our calculations confirm that the *absolute* response time for inline monitoring is slightly worse than that of RIARC in C_M: 116ms vs. 98ms under the Steady, and 182ms vs. 179ms under the Burst workloads respectively. This latency degradation for inline monitoring stems from the $\approx$5µs slowdown induced by the RV analysis, which results in frequent "pausing" of worker processes. Monitors comprising richer analyses produce longer pauses in worker processes, which can degrade the response time further [46, 37, 69].

Table 3 Percentage overhead on C_H (500k) and C_M (5k) w.r.t. baseline at *maximum* workload.

Concurrency	Workload	Response time %		Memory consumption %		Scheduler utilisation %	
		Inline	RIARC	Inline	RIARC	Inline	RIARC
C_H (500k)	Steady	4	95	1	23	0	123
	Burst	55	97	16	56	0	123
C_M (5k)	Steady	246	194	1	8	3	52
	Burst	193	190	1	10	4	50

5.6 Discussion

The RIARC scheduler utilisation in tbl. 3 is higher than the reported values for inline monitoring. This should not be construed as an inefficiency. From a reactive systems perspective, growth in the scheduler utilisation indicates *scalability*, as the low memory consumption in tbl. 3 affirms. RIARC benefits from the ample schedulers to improve the overall system response time *without* overtaxing the system. Indeed, [8, fig. 20 in app. C.6.4] demonstrates that the mean absolute scheduler utilisation in the benchmarks of sec. 5.5 is just $\approx 10\%$ under both the Steady and Burst workloads. Tbl. 3 shows that the reduction in latency makes RIARC comparable to inline monitoring in moderate concurrency scenarios.

Sec. 1 names *responsiveness* as a key reactive systems attribute [94]. RIARC prioritises responsiveness by isolating its monitors into asynchronous concurrent units. This design naturally exploits the available processing capacity of the host platform by maximising monitor *parallelism* when possible. Inline monitoring reaps fewer benefits in identical settings because its lock-step execution with the SuS robs it of potential parallelism gains.

Secs. 5.4.1 – 5.4.3 attest to the impracticality of centralised monitoring for reactive systems. Bottlenecks hinder its ability to scale, compelling it to consume inordinate amounts of memory, which can lead to failure, as sec. 5.4.2 shows. Despite these shortcomings, many RV tools in this setting use centralised monitoring, e.g. [50, 18, 126, 65, 81, 110, 72, 37, 41, 38, 2, 103].

6 Conclusion

Reactive software calls for instrumentation methods that uphold the responsive, resilient, message-driven, and elastic attributes of systems. This is attainable *only if* the instrumentation exhibits these qualities. Runtime verification imposes another demand on the instrumentation: the trace event sequences it reports to monitors must be *sound*, i.e., traces do not omit events and preserve the ordering with which events occur locally at processes.

This paper presents RIARC, a novel decentralised instrumentation algorithm for outline monitors meeting these two demands. RIARC uses outline monitors to decouple the runtime analysis from system components, which minimises latency and promotes *responsiveness*. Outline monitors can fail independently of the system and each other to improve *resiliency*. RIARC gathers events non-invasively via a tracing infrastructure, making it *message-driven* and suited to cases where inlining is inapplicable. The algorithm is *elastic*: it reacts to specific events in the trace to instrument and garbage collect monitors on demand.

Our asynchronous setting complicates the instrumentation due to potential trace event loss or reordering. RIARC overcomes these challenges using a next-hop IP routing approach to rearrange and report events soundly to monitors. We validate RIARC by subjecting its corresponding Erlang implementation to rigorous systematic testing, confirming its correctness. This implementation is validated via extensive empirical experiments. These subject the implementation to large realistic workloads to ascertain its reactiveness. Our experiments show that RIARC optimises its memory and scheduler usage to maintain latency feasible for soft real-time applications. We also compare RIARC to inline and centralised monitoring, revealing that it induces *comparable* latency to inlining under moderate concurrency.

Related work. Other work on inlining besides that cited in sec. 1, e.g. [78, 25, 50, 49, 53], does not separate the instrumentation and runtime analysis. This view is commonplace in monolithic settings, where the instrumentation is often assumed to induce minimal runtime overhead. As a result, many inline approaches focus on the efficiency of the analysis but neglect the instrumentation cost (e.g. [63] attributes overhead solely to the analysis). These arguments for monolithic systems are often ported to concurrent settings. For instance, [107, 126, 29, 46, 125, 66, 21] propose efficient runtime monitoring algorithms but do not account for, nor quantify, the overhead due to gathering trace events. Tools that measure the runtime overhead, such as [41, 37, 19, 34, 72, 133], coalesce the instrumentation and runtime analysis costs, making it difficult to gauge the source of inefficiencies. Some literature [39, 52] even extends the assumption about minimal instrumentation overhead to offline monitoring, stating that the instrumentation consists of "only" capturing trace events. Sec. 5.4.1 shows this *not* to be the case. We are unaware of empirical studies such as ours that concretely distinguish between and quantify the instrumentation and runtime analysis overhead.

Sec. 5.6 remarks that centralised monitoring is used for concurrent runtime verification despite its evident limitations. One plausible reason for this is that the empirical scrutiny of such tools lacks proper benchmarking (e.g. [50, 18, 126, 65, 81]) or uses insufficient workloads that fail to expose the issues of centralised set-ups (e.g. [110, 72, 37, 41, 38, 2, 103]). Gathering inadequate metrics can also bias the interpretation of empirical data; see sec. 5.4.1. Works, such as [38, 19, 34, 124], consider the memory consumption and latency metrics. Our evaluation of inline, centralised, and RIARC monitoring uses (i) *combinations* of hardware and software, with (ii) two concurrency models that test *edge-case* and *general-case* scenarios, under (iii) *high* workloads that go beyond the state of the art, applying (iv) *realistic* workload profiles, interpreted against (v) *relevant* performance metrics that give a multi-faceted view of runtime overhead. To the best of our knowledge, this is generally not done in other studies, e.g. [114, 113, 47, 46, 119, 30, 106, 38, 41, 19, 50, 51, 53, 72, 59, 60, 27, 110, 97, 34].

Outline instrumentation decouples the execution of the SuS and monitor components in space (i.e., isolated threads) and time (i.e., asynchronous messaging). The tracing infrastructure outline instrumentation uses mirrors the publish-subscribe (Pub/Sub) pattern [129]. In this set-up, consumers subscribe to a *broker* that advertises events. Centralised instrumentation follows a Pub/Sub approach: the SuS produces trace events and deposits them into *one* global trace buffer that tracers receive from (see fig. 1b). Despite similarities, e.g. tracers register and deregister with the tracing infrastructure at runtime, RIARC differs from conventional Pub/Sub messaging in three fundamental aspects. Chiefly, Pub/Sub publishers are unaware of the subscribers interested in receiving messages because this bookkeeping task is appointed to the broker. By contrast, next-hop routing relies on knowing the *explicit* address of recipients to forward messages. Furthermore, in Pub/Sub messaging, subscribers do not communicate with publishers, whereas RIARC tracers exchange *direct* detach requests between one another to reorganise the choreography (refer to sec. 3.4). Lastly, Pub/Sub brokers are typically predefined and remain fixed, while trace partitioning *reconfigures* the tracing topology, creating and destroying brokers in reaction to dynamic changes in SuS.

One assumption we make about process tracing is A_4, i.e., tracing gathers the spawn events of parent processes before all the events of child processes. While A_4 induces a partial order over trace events, it is *weaker* than happened-before causality [95], as the events gathered from sets of child SuS processes need not be causally ordered. Demanding the latter condition would entail additional computation on the part of the tracing infrastructure and could increase runtime overhead. Maintaining minimal overhead is critical to our instrumentation because it preserves the responsiveness attribute of reactive systems. Tracing assumption A_4 and the RIARC logic detailed in sec. 3 guarantee trace soundness (def. 1), which suffices for RV monitoring. Since our work targets soft real-time systems [94, 92] scoped in a reliable messaging setting (see sec. 1), we do not tackle the problem of ensuring time-bounded causally-ordered message delivery [20] nor implement exactly-once delivery semantics [83]. We will address these challenges in future extensions of this work.

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