



Uniformity Within Parameterized Circuit Classes

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Abstract

We study uniformity conditions for parameterized Boolean circuit families. Uniformity conditions require that the infinitely many circuits in a circuit family are in some sense easy to construct from one shared description. For shallow circuit families, logtime-uniformity is often desired but quite technical to prove. Despite that, proving it is often left as an exercise for the reader – even for recently introduced classes in parameterized circuit complexity, where uniformity conditions have not yet been explicitly studied. We formally define parameterized versions of linear-uniformity, logtime-uniformity, and FO-uniformity, and prove that these result in equivalent complexity classes when imposed on para-AC^0 and $\text{para-AC}^{0\uparrow}$. Overall, we provide a convenient way to verify uniformity for shallow parameterized circuit classes, and thereby substantiate claims of uniformity in the literature.

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1 Introduction

Circuit complexity theory analyzes problems through the (smallest) size and depth of Boolean circuits that solve them, linking logic, space complexity, and parallel complexity theory [16]. Because a Boolean circuit has a fixed number of inputs, the actual object of study is a circuit family, which contains a circuit for every input length n .

Without restrictions, circuit families are too expressive to be used as a model of computation, as non-uniform circuit families can even express non-computable functions. Hence, uniformity conditions are often imposed to ensure that the circuits in the family are in some sense easy to construct. With uniformity conditions, circuit families are a useful model in the study of, amongst others, parallel and descriptive complexity theory [16].

The main idea behind uniformity conditions is that, for a class of circuit families \mathcal{C} , the structure of a family's circuits themselves should be less complex than the problems that families in \mathcal{C} can solve. For the class of constant-depth circuit families, this line of thinking has led to the very restrictive logtime-uniformity condition, requiring that the edge relation of the circuits in a family must be (simultaneously) decidable in logarithmic time.

Logtime computations are difficult to analyze or work with [11, 16]. Therefore, logtime-uniformity is rarely proved directly, but instead shown using results such as those of Barrington, Immerman, and Straubing [11]. They show that if a constant-depth circuit family is describable in terms of first-order logic, there is another, logtime-uniform constant-depth



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circuit family equivalent with it. Using this correspondence, one can show the existence of a logtime-uniform circuit family without directly dealing with the technical intricacies of logtime computations.

Recently, the interest in circuit complexity was renewed in the setting of parameterized complexity [1, 2, 4, 12, 3]. In parameterized complexity theory, problems are classified on a finer scale with respect to an additional parameter instead of just input size. In the context of circuit complexity this spawns new circuit classes, that identify problems which are in some sense parallel constant time decidable up-to some parameter [2].

Parameterized circuit classes require new parameterized uniformity conditions. Recent works [1, 2, 4, 12, 3] have adapted the logtime-uniformity of Barrington et al., though they are not very specific in their exact definitions. They generally refer to the complexity of computing single bits in the binary encoding of circuits, but it is not specified what the binary encoding is. Additionally, though the literature cites [11], it is not clear if the equivalence results of Barrington et al. carry over to the parameterized circuit classes.

In general, the literature often leaves uniformity claims as an exercise for the reader. To the best of our knowledge, only [1, Theorem 3.2, Appendix A] sets out to prove one of its uniformity claims. However, the proof appears to erroneously assume that logtime-uniformity gives a random-access Turing machine polylogarithmic time to decide the graph structure of the circuits, while it allows only logarithmic time.

■ **Table 1** Informal overview of the parameterized uniformity notions used in the paper.

Condition	Question (for circuit $C_{n,k}$)	Decision complexity
linear-BD-uniform	$\langle \text{local question}, n, k \rangle$	$\text{DTIME}(\log n + f(k))$
logtime-D-uniform	$\langle \text{local question}, \{0, 1\}^n, \{0, 1\}^k \rangle$	$\text{DTIME}^R(\log n + f(k))$
logtime-E-uniform	$\langle \text{path question}, \{0, 1\}^n, \{0, 1\}^k \rangle$	$\text{DTIME}^R(\log n + f(k))$
FO-D-uniform	$\langle \text{local question}, \{0, 1\}^n, \{0, 1\}^k \rangle$	para-FO in parameter k
FO-E-uniform	$\langle \text{path question}, \{0, 1\}^n, \{0, 1\}^k \rangle$	para-FO in parameter k

Contributions. We introduce and analyze uniformity conditions for parameterized circuit complexity. Specifically, we define a suitable notion of the logtime-uniformity used in the literature, and show it to be equivalent to more natural notions when imposed on the shallow parameterized circuit classes para-AC^0 and $\text{para-AC}^{0\uparrow}$.

An overview of the discussed uniformity notions, formally defined in Sections 3 and 5, can be found in Table 1. We consider direct uniformity notions, which require the local structure of circuits to be easily decidable, and extended uniformity notions that also consider paths in the circuit. The direct logtime-D-uniformity is based on logtime-DCL-uniformity introduced in [11] and used in the reference work [16]. We believe our definition captures the more informal notions of parameterized logtime-uniformity found in [1, 2, 4, 12, 3]. For the classes para-AC^0 and $\text{para-AC}^{0\uparrow}$, we show that these notions are equivalent to linear-BD-uniformity, a parameterized variant of U_D -uniformity from [14]. We introduce a parameterized variant of FO-uniformity from [11], and show that this too is equivalent to our earlier notions when applied to para-AC^0 and $\text{para-AC}^{0\uparrow}$. Finally, we also show this for strict adaptations of extended logtime and first-order uniformity.

Our results allow for an easier analysis of uniformity for shallow parameterized circuit classes, and address uniformity claims in the literature.

Outline. Section 2 contains preliminaries on circuit complexity and known uniformity results. In Section 3, we formally define the direct uniformity conditions roughly described in Table 1. In Section 4, we show that imposing these different conditions leads to the same complexity class, both for para-AC^0 and $\text{para-AC}^{0\uparrow}$. In Section 5, we show that this also holds for strict adaptations of extended uniformity conditions. In Section 6, we show how our work can be related to the descriptive complexity-based work on uniformity for $\text{AC}[t(n)]$.

2 Preliminaries

In this section, unless otherwise noted, standard definitions in circuit complexity and parameterized complexity are based on the reference works [16] and [7] respectively.

2.1 Circuit families

A **circuit family** is a set of (Boolean) circuits $\{C_n : n \in \mathbb{N}\}$ such that C_n has n input gates (fan-in 0) and at least one output gate (fan-in 1, fan-out 0). The remaining (**internal**) gates are AND, OR, or NOT gates. A circuit's **size** is the number of gates in it, and its **depth** the length of the longest (input to output) path it contains. The size and depth of a circuit family C are functions s, d , where $s(n), d(n)$ are equal to the size and depth of C_n respectively.

We generally care about circuit families in which each circuit has one output gate. We then define the language recognized by the circuit family C as $\{x \in 2^* : C_{|x|}(x) = 1\}$. That is, given some binary string x , we take the circuit $C_{|x|}$ with $|x|$ input gates, set the input gates to the bits of x , and evaluate it. The word is accepted if and only if the output gate evaluates to 1. More generally, a circuit with n inputs and m outputs induces a binary function $2^n \rightarrow 2^m$. Circuit families induce a function $2^* \rightarrow 2^*$.

The **circuit class** AC^0 consists of all languages that are recognized by polynomially sized circuit families of constant depth. That is, Q is in AC^0 if there is a circuit family C with size $s(n) = O(n^c)$ and depth $d(n) = O(1)$, such that $Q = \{x : C(x) = 1\}$. It is important to note that all gates have unbounded fan-out, and the AND and OR gates unbounded fan-in.

2.2 Parameterized complexity

Parameterized complexity theory studies computational problems modulo (pre)computations on some input-based parameter. The parameter function is considered part of the problem.

► **Definition 1.** A **parameterized problem** (Q, κ) consists of a language $Q \subseteq 2^*$ and a **polynomial-time computable parameter function** $\kappa : 2^* \rightarrow \mathbb{N}$.

We follow the literature on shallow parameterized circuit complexity [5, 1] in additionally requiring κ to be FO-computable [9, Definition 2.5], equivalently that κ can be computed by a logtime-D-uniform circuit family of polynomial size and constant depth (cf. Definition 8). This requirement can be removed by modifying the definition of para-FO to being given $f(\kappa(x))$ as a precomputed value, as discussed in the full version (Appendix A).

Parameterized classes are often defined in terms of non-parameterized classes.

► **Definition 2** ([6]). Let \mathcal{X} be a complexity class. A **parameterized problem** (Q, κ) is in $\text{Para}(\mathcal{X})$ if and only if there is a computable function f with $\{\langle x, f(\kappa(x)) \rangle : x \in Q\}$ in \mathcal{X} .

Classes such as parameterized linear time can also be given more explicitly.

► **Definition 3.** We write $\text{DTIME}(t(n) + f(k))$ for the class of parameterized problems (Q, κ) for which there is a multitape Turing machine that solves $x \in Q$ in $O(t(|x|) + f(\kappa(x)))$ time.

The difference in style between these definitions lies in whether the precomputation is part of the input or given implicitly by means of extra time. In [6], it is shown that (Q, κ) is in $\text{DTIME}(t(n) + f(k))$ for some computable f if and only if (Q, κ) is in $\text{para-DTIME}(t(n))$, but there are no such results for the sublinear random-access Turing machines we use later.

2.3 Parameterized circuit complexity

Parameterized circuit complexity studies classes $\text{Para}(\mathcal{X})$ for ordinary circuit complexity classes \mathcal{X} , as well as other classes defined in terms of parameterized circuit families.

► **Definition 4** ([1]). *A parameterized circuit family C is a set $\{C_{n,k} : n, k \in \mathbb{N}\}$ of circuits, such that each $C_{n,k}$ has n input gates. A parameterized problem (Q, κ) is decided by C if $x \in Q \iff C_{|x|, \kappa(x)}(x) = 1$ holds. Size and depth are now functions $s(n, k)$ and $d(n, k)$.*

The parameterized circuit class para-AC^0 is defined as the parameterized problems solved by constant-depth parameterized circuit families of size $O(f(k)n^c)$, where f is again some computable function that varies per circuit family. The class $\text{para-AC}^{0\uparrow}$ is defined in terms of $O(f(k)n^c)$ -sized circuits with depth $O(f(k))$ [1]. $\text{Para}(\text{AC}^0)$ is equal to para-AC^0 [5].

2.4 Uniformity

Uniformity conditions for shallow circuit classes are defined in terms of connection languages. These languages express the connections between the gates in the circuit family. To achieve this goal, the gates in each circuit are first identified by a numbering.

► **Definition 5.** *An admissible numbering of a circuit family $C = \{C_n : n \in \mathbb{N}\}$ of size $s(n)$ assigns a number to every gate in C so that:*

1. *within each C_n , no two gates have the same number,*
2. *the n input gates of C_n are numbered from 0 to $n - 1$,*
3. *the m output gates of C_n are numbered from n to $n + m - 1$, and,*
4. *gates in C_n are numbered polynomially in $s(n)$, that is, with numbers of $O(\log s(n))$ bits.*

To improve readability, we will assume that circuit families come with fixed admissible numberings (which we may choose freely), and often identify gates with their gate number.

► **Definition 6** ([11, 14]). *Let C be a circuit family. The direct connection language $L_D(C)$ consists of all strings of the form $\langle G, a, p, z \rangle$ where, writing n for $|z|$:*

1. *G is a gate in C_n ;*
2. *if $p = \epsilon$ then $a < 3$ indicates the type of G (one of AND, OR, NOT);*
3. *otherwise, the p th gate feeding into G is a .*

The binary direct connection language $L_{BD}(C)$ consists of all strings of the form $\langle G, a, p, n \rangle$ satisfying the same conditions, now with n written in binary. That is:

$$L_{BD}(C) = \{\langle G, a, p, |z| \rangle : \langle G, a, p, z \rangle \in L_D(C)\}.$$

There is also an extended connection language $L_E(C)$, wherein p can also be a path. We will come back to this in Section 5. The encoding of the lists $\langle \dots, \dots \rangle$ in Definition 6 is addressed in Section 2.6. First, we introduce three direct uniformity notions, defined in terms of the decision complexity of direct connection languages.

Linear-time. In [14], Ruzzo introduced uniformity conditions for shallow circuit classes. The following definition is based on Ruzzo's U_D -uniformity.¹

► **Definition 7.** A circuit family C is **linear-BD-uniform** if $L_{BD}(C)$ is in $\text{DTIME}(n)$.

That is, a deterministic multitape Turing machine can decide $w \in L_{BD}(C)$ in time $O(|w|)$.

Logtime. Later uniformity notions were based on random-access Turing machines. A **random-access Turing machine** [16, Appendix A4] is a multitape Turing machine equipped with a special query tape and query state. Whenever the machine enters the query state, it obtains the value of the a th bit on the input tape, where a is the binary address written on the query tape, or an out-of-bounds response if a is beyond the length of the input (or not a number). Importantly, the query tape is not erased on query, and the input tape is read-only.

We write $\text{DTIME}^R(t(n))$ for the class of problems that can be solved in $O(t(n))$ time by a random-access Turing machine, and define $\text{DTIME}^R(t(n) + f(k))$ analogously to Definition 3.

► **Definition 8** ([11]). Circuit family C is **logtime-D-uniform** if $L_D(C)$ is in $\text{DTIME}^R(\log n)$.

Logtime-D-uniformity is arguably the most well-known uniformity condition for AC^0 . Yet not much is known about $\text{DTIME}^R(\log n)$. Clearly $\text{DTIME}^R(\log n) \subseteq \text{DTIME}(n \log n)$ [13], but it is to the best of our knowledge unknown whether this is strict. As far as we know, it is for example also open whether a random-access Turing machine can multiply two m -bit numbers in $O(m)$ time. What is known is that they can add m -bit numbers in $O(m)$ time, and determine the length of their input in $O(\log n)$ time [11, Lemma 6.1].

First-order definable. The class **FO** consists of the languages that are first-order definable in the predicates \leq and **Bit**. That is, they are defined by a first-order sentence using symbols from $\{\forall, \wedge, \neg, \leq, \text{Bit}, X\}$ as follows [11, 9]. A word w induces a first-order structure S_w whose domain consists of the numbers 0 to $|w|$, where: \leq is interpreted as the standard order on natural numbers, $\text{Bit}(i, j)$ is true if and only if the i th bit of j is 1, and $X(i)$ is true if and only if the i th bit of w is 1. A sentence ϕ then defines the language $\{w : S_w \models \phi\}$.

We may assume that the language also contains ternary predicates for addition and multiplication, as they are first-order definable in \leq and **Bit** [11, 9]. We may also assume that it contains a constant symbol for the length of the input, and that we may quantify over (the binary representations of) numbers below $O(|w|^c)$, by using $O(c)$ variables [11, p. 293].

► **Definition 9** ([11]). A circuit family C is **FO-D-uniform** if $L_D(C)$ is in **FO**.

For polynomially-sized circuit families, it can be shown that linear-BD-uniformity implies logtime-D-uniformity, which in turn implies FO-D-uniformity. FO-D-uniformity is easier to work with than logtime-D-uniformity. In fact, there are many examples of languages for which the natural circuit families deciding them are quickly seen to be FO-D-uniform, but for which it is unknown whether they are logtime-D-uniform or linear-BD-uniform.

► **Example 10.** Consider problem $X = \{x : \text{the } \lfloor \sqrt{|x|} \rfloor \text{th bit of } x \text{ is } 1\}$. It is easy to see that X is in AC^0 : there is a circuit family C where each C_n consists of essentially one wire from the $\lfloor \sqrt{n} \rfloor$ th input gate to the output gate. It has only one admissible numbering, and its direct connection language is $\{\langle n, \lfloor \sqrt{n} \rfloor, 0, z \rangle : |z| = n\}$.

¹ Ruzzo requires $\text{DTIME}(\log s(n))$ on a slightly different language, but this is equivalent for our cases.

The most difficult part in showing that this family is uniform is to show that we can somehow identify $\lfloor \sqrt{n} \rfloor$. For FO-D-uniformity, this is easy: $r = \lfloor \sqrt{n} \rfloor$ is defined by the formula $r \cdot r \leq n \wedge (\forall s > r) s \cdot s > n$. Showing that C is logtime-D-uniform appears to be more difficult, and we do not know whether this is the case. It is likely not linear-BD-uniform, as multiplication is conjectured to not be linear-time computable [8]. \lrcorner

2.5 Uniform AC^0

Rather than the uniformity of specific circuit families, we are usually more interested in whether an equivalent uniform family exists for the same complexity class.

► **Convention.** Let \mathcal{U} be a uniformity condition, and \mathcal{C} a class of (parameterized) circuit families. If \mathcal{X} is defined as the class of problems solved by families in \mathcal{C} , then \mathcal{U} -uniform \mathcal{X} is the subclass of problems solved by \mathcal{U} -uniform families in \mathcal{C} .

From this perspective, uniformity conditions can be shown to be equivalent for AC^0 .

► **Theorem 11** (Barrington, Immerman, Straubing [11]). *The following classes are equal:*

1. logtime-D-uniform AC^0
2. FO-D-uniform AC^0
3. FO

On the way to our main results we prove the following folklore extension of Theorem 11.

► **Theorem 12.** *Linear-BD-uniform AC^0 equals logtime-D-uniform AC^0 .*

A stronger version, that logtime-D-uniformity is even equivalent with linear-BD-uniformity, is stated in [13, Section 4] and appears to be used implicitly in other work [15, Section 1.1]. However, this is not something we can prove. The argument in [13] seems to silently assume that $DTIME^R(n) = DTIME(n)$ which we believe is an open problem.

We stress that the results above do not show that the uniformity conditions are equivalent. In particular, $DTIME^R(\log n)$ is strictly weaker than FO. It merely happens to be the case that the extra power of FO for constant-depth circuit family descriptions does not lead to circuit families with more computational power than any logtime-uniform circuit family.

2.6 Encoding lists

We define an encoding for the lists in Definition 6 as a generalization of the 2-tuple encoding used by Barrington et al. [11]. Each element $x \in 2^*$ is coded as $\delta(|x|)01x$, where $\delta(|x|)$ encodes the length of x in base $\{00, 11\}$ and 01 acts as a separator.

► **Definition 13.** *We encode $\langle x_0, \dots, x_m \rangle$ as*

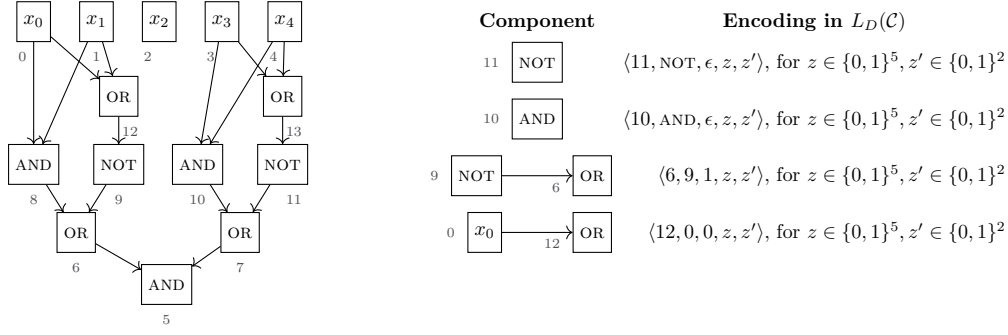
$$\delta(|x_0|)01x_0 \delta(|x_1|)01x_1 \dots \delta(|x_m|)01x_m$$

and define projection functions $\pi_i : 2^* \rightarrow 2^*$ by

$$\pi_i(x) = \begin{cases} x_i & \text{if } x \text{ is of the form } \langle x_0, \dots, x_m \rangle \text{ with } i \leq m, \text{ and} \\ 0 & \text{otherwise.} \end{cases}$$

For example, $\langle 0, 00, 000 \rangle$ is encoded as

$$\underbrace{11}_{\delta(|x_0|)} 01 \underbrace{0}_{x_0} \underbrace{1100}_{\delta(|x_1|)} 01 \underbrace{00}_{x_1} \underbrace{1111}_{\delta(|x_2|)} 01 \underbrace{000}_{x_2}.$$



■ **Figure 1** The circuit $C_{5,2}$ from the family C , and associated words $w \in L_D(C)$.

The encoding can be worked with in linear time, in random-access logarithmic time, and in first order logic with ordering and Bit. In particular, it can be checked whether a string encodes a list, the lengths of list items can be extracted, and the projection functions can be computed, provided that the relevant item is not too long (a logtime-machine cannot retrieve items of superlogarithmic length). Details can be found in the full version (Appendix B).

2.7 Parameterized uniformity

In [3, Proposition 6], Chen and Flum prove a uniform version of $\text{para-AC}^0 = \text{Para}(\text{AC}^0)$. Their proof carries over to our setting of parameterized linear-BD-uniformity we define in Section 3 as follows. In our reformulation we use that parameter functions κ are FO-computable.

► **Theorem 14** ([3]). *Linear-BD-uniform para-AC^0 is equal to $\text{Para}(\text{linear-BD-uniform } \text{AC}^0)$.*

3 Direct parameterized uniformity

We first define uniformity notions for parameterized circuit families. Admissible numberings (Definition 5) carry over to parameterized circuit families in the straightforward way, and we again assume each parameterized family to come with such a numbering.

► **Definition 15.** *Let C be a parameterized circuit family. The **direct connection language** $L_D(C)$ consists of all strings of the form $\langle G, a, p, z, z' \rangle$ where, writing n for $|z|$ and k for $|z'|$:*

1. G is a gate in $C_{n,k}$;
2. if $p = \epsilon$ then $a < 3$ and indicates the type of G (one of AND, OR, NOT);
3. otherwise, the p th gate feeding into G is the gate numbered a .

The **binary direct connection language** $L_{BD}(C)$ consists of all strings of the form $\langle G, a, p, n, k \rangle$ satisfying the same conditions, now with n and k written in binary. That is:

$$L_{BD}(C) = \{ \langle G, a, p, |z|, |z'| \rangle : \langle G, a, p, z, z' \rangle \in L_D(C) \}.$$

► **Example 16.** Consider the language

$$L = \{ x_0 \dots x_{n-1} \mid \forall i \in [1, \lfloor \sqrt{n} \rfloor]. x_0 = x_{i-1} \text{ and } x_{n-i} = x_{n-1} \}.$$

Figure 1 shows the circuit $C_{5,2}$ from the circuit family C that computes the parameterized problem (L, κ) , where the parameter function is defined by $\kappa(x) = \lfloor \sqrt{|x|} \rfloor$, together with some words from the direct connection language $L_D(C)$. ─

We now define uniformity conditions for parameterized circuit families. These are based on non-parameterized uniformity conditions. The difference is that parameterized uniformity conditions allow a precomputation on the same parameter function used for the circuit family. That is, where before we had $t(n)$ time to decide connections in circuits C_n , we now have $t(n) + f(k)$ time to decide connections in circuits $C_{n,k}$, for a computable f of choice.

We also adapt FO-D-uniformity. Write para-FO for Para(FO). The motivation for FO-D-uniformity for parameterized circuit families is that words $\langle G, a, p, z, z' \rangle$ relating to $C_{|z|, |z'|}$ should now be first-order expressible in terms of $|z|$ and $f(|z'|)$, where f is a computable function of choice. Again writing π_4 for the fifth projection function (so that $\pi_4(\langle G, a, p, z, z' \rangle) = z'$), this can equivalently be expressed as $(L_D(C), \pi_4)$ being in para-FO.

► **Definition 17.** *Let C be a parameterized circuit family. We call it*
linear-BD-uniform *if $(L_{BD}(C), \pi_4)$ is in $\text{DTIME}(n + f(k))$ for some computable f , that is, on inputs w of the form $\langle G, a, p, n, k \rangle$ it takes time $O(|w| + f(k))$;*
logtime-D-uniform *if $(L_D(C), \pi_4)$ is in $\text{DTIME}^R(\log n + f(k))$ for some computable f , that is, on inputs w of the form $\langle G, a, p, z, z' \rangle$ it takes time $O(\log |w| + f(|z'|))$;*
FO-D-uniform *if $(L_D(C), \pi_4)$ is in para-FO.*

In the following, we sometimes leave the parameter function π_4 implicit and e.g. simply state that linear-BD-uniformity is defined as $L_{BD}(C)$ being in $\text{DTIME}(n + f(k))$.

For parameterized circuit families of size $O(f(k)n^c)$, linear-BD-uniformity implies logtime-D-uniformity, which in turn implies FO-D-uniformity. The former can be shown as follows.

► **Lemma 18.** *Let C be a parameterized circuit family of size bounded by $f(k)n^c$. If C is linear-BD-uniform then C is logtime-D-uniform.*

Proof sketch. Let M be a machine deciding $(L_{BD}(C), \pi_4)$ in time $O(n + f(k))$, and consider the following random-access Turing machine M' : it rejects all inputs not of the form $\langle G, a, p, z, z' \rangle$ with $|G|, |a|, |p|$ below $O(\log |z| + f(|z'|))$. Otherwise, it writes $\langle G, a, p, |z|, |z'| \rangle$ on a work tape and then acts as M . Now M' witnesses $(L_D(C), \pi_4) \in \text{DTIME}^R(\log n + g(k))$. A full proof can be found in the full version (Appendix B). ◀

Next we prove that logtime-D-uniformity implies FO-D-uniformity. It suffices to show the inclusion $\text{DTIME}^R(\log n + f(k)) \subseteq \text{para-FO}$ for all computable f . We do this by first showing that $\text{DTIME}^R(\log n + f(k))$ is contained in linear-BD-uniform para- AC^0 , because this will be used again in Section 4.2. Through Theorems 11 and 12, the following result (and proof) can be seen as a parameterized variant of $\text{DTIME}^R(\log n) \subseteq \text{FO}$ shown in [11, Proposition 7.1].

► **Lemma 19.** *$\text{DTIME}^R(\log n + f(k))$ is contained in linear-BD-uniform para- AC^0 , for all computable f .*

Proof sketch. A random-access machine M can make at most $O(\log n + f(k))$ queries in $O(\log n + f(k))$ time, so a constant depth circuit family of size $2^{O(\log n + f(k))} = O(g(k)n^c)$ can nondeterministically branch over all series of query responses, verify which is correct (checking all queries in parallel), and propagate the output of a simulation of M on the correctly guessed responses to the output gate. This can be done linear-BD-uniformly because simulating an $O(\log n + f(k))$ time random-access Turing machine by answering queries from a given list of guesses takes $O(\log n + h(k))$ time on a non-random-access Turing machine.

A full proof can be found in the full version (Appendix B). ◀

We are now ready to prove that logtime-D-uniformity implies FO-D-uniformity. Here we can make use of the work of Barrington et al. [11] and that of Chen and Flum [3].

► **Lemma 20.** *Let C be a parameterized circuit family of size bounded by $f(k)n^c$. If C is logtime-D-uniform then C is FO-D-uniform.*

Proof. Assume C is logtime-D-uniform. Then, by definition, there is some computable g so that $(L_D(C), \pi_4)$ is in $\text{DTIME}^R(\log n + g(k))$. From the inclusions

$$\begin{aligned} \text{DTIME}^R(\log n + g(k)) &\subseteq \text{linear-BD-uniform para-AC}^0 && \text{by Lemma 19} \\ &= \text{Para}(\text{linear-BD-uniform AC}^0) && \text{by Theorem 14} \\ &= \text{Para}(\text{FO}) && \text{by Theorems 11 and 12} \\ &= \text{para-FO} && \text{by definition} \end{aligned}$$

it follows that $(L_D(C), \pi_4)$ is in para-FO, meaning that C is FO-D-uniform. ◀

4 Uniform para-AC⁰ and para-AC^{0†}

In the previous section we have seen that, for parameterized circuit families of size $f(k)n^c$, linear-BD-uniformity implies logtime-D-uniformity, which in turn implies FO-D-uniformity. It is unknown whether any of these the implications can be reversed. (See also Example 10.)

We can however show implications up-to similar-size circuit equivalence in the reverse direction, by which we mean that the uniformity conditions do not result in different complexity classes for both para-AC⁰ and para-AC^{0†}. That is, for every FO-D-uniform $O(f(k)n^c)$ -sized circuit family of depth $O(d(k))$, there is a linear-BD-uniform $O(g(k)n^b)$ -sized family of depth $O(d(k))$ that decides the same parameterized problem.

For para-AC⁰, the equality of logtime-D-uniform para-AC⁰ and FO-D-uniform para-AC⁰ mirrors Theorem 11, and could be proved using the constant-depth techniques in [11]. This does not work for the $f(k)$ depth circuits of para-AC^{0†} (the circuits blow up). We address this by constructing logtime-uniform circuits of $f(k)$ layers that simulate FO-uniform circuits by computing their connection language. A similar layered approach can be found in [10], where they simulate FO[$t(n)$] to prove uniformity equivalences for AC[$t(n)$].

► **Theorem 21.** *The following classes are equal:*

1. linear-BD-uniform para-AC^{0†},
2. logtime-D-uniform para-AC^{0†}, and
3. FO-D-uniform para-AC^{0†}.

The same holds for para-AC⁰.

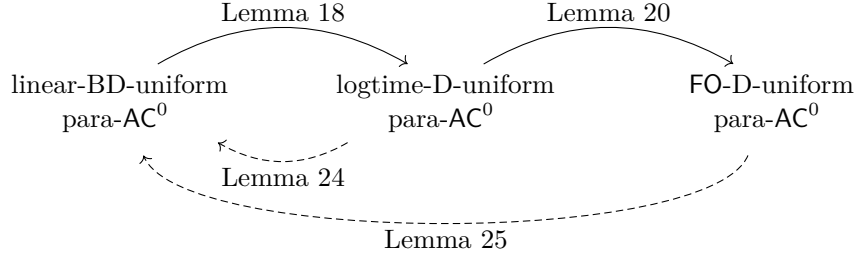
Proof outline. We will use the following structure, as visualized in Figure 2 for para-AC⁰. In Section 3, we have already proved that

$$\text{linear-BD-uniformity} \xrightarrow{\text{Lemma 18}} \text{logtime-D-uniformity} \xrightarrow{\text{Lemma 20}} \text{FO-D-uniform}$$

for circuit families of size $O(f(k)n^c)$, which directly gives the inclusions $(1) \subseteq (2) \subseteq (3)$ for both para-AC⁰ and para-AC^{0†}. The next step is to prove $(2) \subseteq (1)$, in particular that linear-BD-uniform para-AC⁰ is equal to logtime-D-uniform para-AC⁰ (Lemma 24). We then use this to show $(3) \subseteq (1)$ for both para-AC⁰ and para-AC^{0†} (Lemma 25).

The new inclusions will be proved by simulation. We will show that there are linear-BD-uniform constant-depth circuit families for deciding the connection language $L_D(C)$ of logtime-D-uniform and FO-D-uniform circuit families C of size $O(f(k)n^c)$. We then compose them into larger linear-BD-uniform circuit families to simulate C itself.

To prove that these compositions are indeed linear-BD-uniform, we first show that the class of linear-BD-uniform circuit families is in some sense closed under substitution.



■ **Figure 2** Visualization of the steps in the proof of Theorem 21 for para-AC^0 . Solid arrows are direct implications on the level of circuit families, dashed arrows indicate implications up-to similar-size circuit equivalence. Lemma 24 is used to prove Lemma 25. The proof for $\text{para-AC}^{0\uparrow}$ follows the same structure.

4.1 Substitution

A main ingredient of our construction is that within linear-BD-uniformity we are able to *compose* circuit families. That is, given uniform circuit families A and B , we can uniformly replace some of the gates in A by circuits from B . This can be formalized as follows.

► **Definition 22.** Let A, B be parameterized circuit families, let $M(G, n, k) : \mathbb{N}^3 \rightarrow 2$ be a function marking internal gates in $A_{n,k}$, and let $\text{In}(G, n, k)$ be the fan-in of gate G in $A_{n,k}$. The **substitution** $A[B/M]$ is the parameterized circuit family where $A[B/M]_{n,k}$ consists of subcircuits $C(G)$ for each gate G in $A_{n,k}$ so that

1. $C(G) = G$ if $M(G, n, k) = 0$,
 2. $C(G) = B_{\text{In}(G, n, k), k}$ if $M(G, n, k) = 1$ (input and output gates become unary OR gates),
 3. and if H is the i th input of G in $A_{n,k}$, then $C(H)$ is the i th input of $C(G)$ in $A[B/M]_{n,k}$.
- That is, $A[B/M]_{n,k}$ is obtained from A by replacing all marked gates with circuits of B .

It can be shown that $A[B/M]$ is linear-BD-uniform if both A and B are, and in addition M and In are reasonably computable.

► **Lemma 23.** Let A, B be linear-BD-uniform parameterized circuit families of size $O(f(k)n^c)$ for some computable f . Let $M(G, n, k) : \mathbb{N}^3 \rightarrow 2$ be a function marking internal gates in $A_{n,k}$, and let $\text{In}(G, n, k)$ be the fan-in of gate G in $A_{n,k}$.

Now $A[B/M]$ is linear-BD-uniform, provided that there is a computable h such that:

- (1) $M(G, n, k)$ is computable in time $|G| + |n| + h(k)$, and
- (2) if $M(G, n, k) = 1$ then $\text{In}(G, n, k)$ is computable in time $|G| + |n| + h(k)$.

Proof sketch. It suffices to define an admissible numbering for $D = A[B/M]$, and show that, under this numbering, $(L_{BD}(D), \pi_4)$ is in $\text{DTIME}(n + f(k))$ for some computable f .

Give unmarked internal gates G in $A_{n,k}$ number $\langle 0, G \rangle$ in $D_{n,k}$. If G is a marked gate and G' is a gate in the circuit $B_{\text{In}(G, n, k), k}$ replacing it, number it $\langle G, G' \rangle$ in $D_{n,k}$. This numbering based on admissible numberings of A and B leads to an admissible numbering of D (cf. Definition 5). An $O(n + f(k))$ -time algorithm deciding $(L_{BD}(D), \pi_4)$ is then obtained from M , In , and $O(n + g(k))$ -time algorithms for $L_{BD}(A)$ and $L_{BD}(B)$ witnessing the linear-BD-uniformity of A and B . A full proof can be found in the full version (Appendix B). ◀

We do not know whether the logtime-D-uniform (parameterized) circuit families are closed under substitution, for reasonable assumptions on M and In . It appears that two random-access Turing machines P, Q are not easily composed without a runtime overhead. For example, computing $P(x_r)$ on input $x = \langle x_l, x_r \rangle$ seems to require offsetting each query

that P makes by an $O(|x_l|)$ offset which, if done naively, adds an $O(\log |x_l|)$ overhead to every query. These naive combinations of two logtime random-access Turing machines can result in $\Omega((\log n)^2)$ -time random-access Turing machines, instead of logtime.

4.2 Simulation

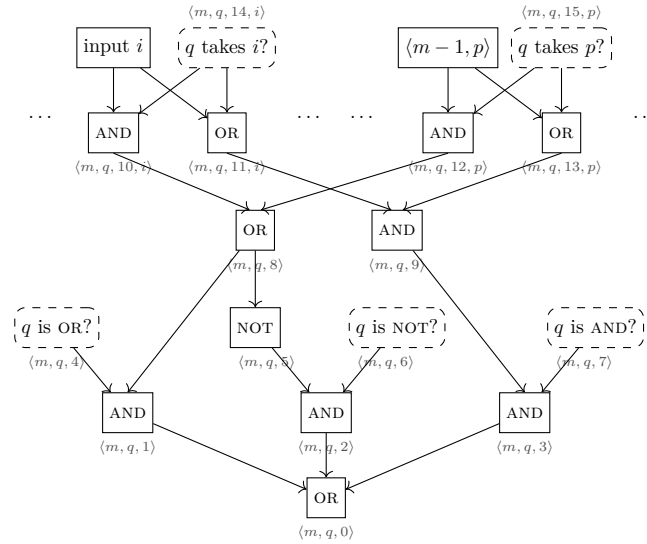
We are now ready to prove Theorem 21 according to the outline given at the start of the section. The first step is the indirect inclusion from logtime-D-uniformity to linear-BD-uniformity.

► **Lemma 24.** *Let C be a parameterized circuit family of size $O(f(k)n^c)$ and depth bounded by $d(k)$, with f, d computable. If C is logtime-D-uniform, there is an equivalent linear-BD-uniform family D of size $O(f'(k)n^{c'})$ and depth $O(d(k))$, with f' computable.*

Proof. Let a be a constant and h a computable function so that for all n, k we have that $N(n, k) = 2^{a \log n + h(k)}$ is greater than any gate number in $C_{n,k}$ (cf. Definition 5). Then the binary representation of $N(n, k)$ is computable in $O(\log n + g(k))$ time without random access for some computable g .

We describe a linear-BD-uniform circuit family D equivalent with C . Circuit $D_{n,k}$ consists of its input gates, $d(k)$ layers of $N(n, k)$ subcircuits we call **simgates**, and one final subcircuit that forwards the correct simgate to the output gate. Every simgate of layer $m+1$ takes all simgates of layer m as input, together with the input gates. We number the q th simgate in layer m with $\langle m, q \rangle$, and the idea is that simgate $\langle m, q \rangle$ in $D_{n,k}$ approaches (monotonically) gate q in $C_{n,k}$, so that, by layer $d(k)$, simgate $\langle d(k), q \rangle$ correctly simulates gate q in $C_{n,k}$.

See Figure 3 for the internals of a simgate. In order to approach gate q of $C_{n,k}$, simgate $\langle m, q \rangle$ queries $L_D(C)$ to select the simgates $\langle m-1, p \rangle$ where p feeds into q in $C_{n,k}$, and the input gates i where input gate i feeds into q in $C_{n,k}$. It also queries $L_D(C)$ to determine whether q is an AND, OR, or NOT gate, and simulates that action on its selected inputs. (By our construction in Figure 3, if $q < N(n, k)$ is not a gate in $C_{n,k}$ then simgate $\langle m, q \rangle$ outputs 0, but it has no influence on the output of $D_{n,k}$, because it is never selected.)



■ **Figure 3** The internals of simgate $\langle m, q \rangle$ simulating gate q of $C_{n,k}$, annotated with an admissible numbering. It takes the n input gates and the $N(n, k)$ simgates of the previous layer as input. The boxes with rounded corners represent subcircuits that determine how to simulate q by querying $L_D(C)$. If there is no gate numbered q in $C_{n,k}$, then the output of the simgate is 0.

Assume for now that components of simgates can directly answer membership queries for $L_D(C)$. In this case the construction shows that they select their input as described above, and perform the action of q (if q is a gate in $C_{n,k}$). Then by induction, for every gate q in $C_{n,k}$, the simgate $\langle d(k), q \rangle$ in the final layer will have the same output as q .

To see this, first observe that by our assumption, the output of $\langle m+1, q \rangle$ is the same as that of q if for all internal gates p that feed into q , the output of $\langle m, p \rangle$ is equal to that of p . Define the **level** of a gate to be the length of the longest path from it to an input gate. The output of simgates $\langle m, q \rangle$ is the same as that of q if the level of q is below m . This can be shown by induction based on the following: (1) If q has level 1 in $C_{n,k}$, then q only takes input gates, and by our observation simgates $\langle m, q \rangle$ have the same output as q for all $m \geq 1$. (2) If q has level $m+1$ and simgates $\langle m', p \rangle$ have the same output as p for all p of lower level and $m' \geq m$, then by our observation $\langle m'', q \rangle$ has the same output as q for all $m'' \geq m+1$.

Finally, to make $D_{n,k}$ behave as desired, it should feed into the output gate the output of simgate $\langle d(k), q \rangle$ for the gate q that feeds into the output gate in $C_{n,k}$. This is the role of the final subcircuit mentioned at the start of the proof. It takes all simgates in the final layer as input, and queries $L_D(C)$ to propagate the output of the correct $\langle d(k), q \rangle$.

The circuits $D_{n,k}$ have very regular structure. Each $D_{n,k}$ is essentially a matrix of $d(k)$ layers of $N(n, k)$ simgates, and each simgate gets all the simgates of the previous layer as input together with the input gates. Apart from the rounded query blocks, the internals of the simgates are also easily seen to be linear-BD-uniform, using for example the admissible numbering in Figure 3. It remains to show how the queries in the simgates are implemented.

Simgate queries. The $L_D(C)$ queries represented by the dashed query blocks in Figure 3 can be implemented by plugging in linear-BD-uniform circuits for $L_D(C)$. A constant-depth linear-BD-uniform circuit family E deciding $L_D(C)$ exists by Lemma 19, and its circuits can be substituted in linear-BD-uniformly by Lemma 23. It is left to prove that the circuits can be given the appropriate query inputs in a linear-BD-uniform way.

For now, we work with the circuit family D' in which the circuits of E have not yet been substituted. Here gates $\langle m, q, 4 \rangle$ (cf. Figure 3) are just AND gates that will be replaced with circuits from E later to obtain D from D' . We add constant circuits V_0 and V_1 to every $D'_{n,k}$, where V_0 has the constant output 0, and V_1 is constant 1. The circuit of E replacing $\langle m, q, 4 \rangle$ should decide whether gate q in $C_{n,k}$ is an OR gate. This can be achieved by giving gate $\langle m, q, 4 \rangle$ the input $I = \langle q, 1, \epsilon, 1^n, 1^k \rangle$. That is, in terms of connection languages, we want $w = \langle \langle m, q, 4 \rangle, V_b, i, n, k \rangle \in L_{BD}(D')$ if and only if the i th bit of I is b . It can be verified that, given such w , the i th bit of I can be decided in time $|w| + g(k)$ for some computable g , and so these queries can be answered in time $|w| + g(k)$ as required for linear-BD-uniformity.

This addresses the type-queries in the simgates. The other queries, those asking whether (input) gate p feeds into q in $C_{n,k}$, are handled similarly, with a small complication: checking whether p feeds into q can be reduced to checking whether p is the i th input of q for any $i \leq N(n, k)$, so the dashed blocks in Figure 3 corresponding to this type of query are actually OR gates over $N(n, k)$ gates that will be substituted by circuits of E , where the i th gate will be given an $L_D(C)$ -query to determine whether p is the i th input of q .

In summary: the queries in the simgates are implemented by hard-wiring $L_D(C)$ -queries into the query blocks in a linear-BD-uniform manner, and then substituting in a linear-BD-uniform circuit family E that decides $L_D(C)$ to answer them. The resulting circuit family D is linear-BD-uniform by Lemma 23, and is equivalent with C by design. ◀

Theorem 12 (mentioned in Section 2.5) can be proved similarly. Using simgates, we can now also prove the following.

► **Lemma 25.** *Let C be a parameterized circuit family of size $O(f(k)n^c)$ and depth bounded by $d(k)$, with f, d computable. If C is FO-D-uniform, there is an equivalent linear-BD-uniform family D of size $O(f'(k)n^{c'})$ and depth $O(d(k))$, with f' computable.*

Proof. By the FO-D-uniformity of C , we have $(L_D(C), \pi_4) \in \text{Para}(\text{FO})$. Theorem 11 gives that $(L_D(C), \pi_4)$ is in $\text{Para}(\text{logtime-D-uniform } \text{AC}^0)$, which by Theorem 14 is equal to $\text{logtime-D-uniform para-AC}^0$. Hence, by Lemma 24, $(L_D(C), \pi_4)$ is in linear-BD-uniform para- AC^0 . The rest of the proof is now the same as for Lemma 24, using a simgate-construction of $d(k)$ layers, and answering $L_D(C)$ -queries in the simgates by substituting in a family witnessing that $(L_D(C), \pi_4)$ is in linear-BD-uniform para- AC^0 . ◀

We have now proved our main result.

Proof of Theorem 21. For both para- AC^0 and para- $\text{AC}^{0\uparrow}$, Item (1) implies Item (2) by Lemma 18, and (2) implies (3) by Lemma 20. Finally, Item (3) implies Item (1) by Lemma 25. (For para- AC^0 , the last implication is obtained from Lemma 25 by setting $d(k) = O(1)$.) ◀

We can also observe the following, which suggests that FO-D-uniformity is not too coarse for para- $\text{AC}^{0\uparrow}$. (This mirrors that (FO-uniform AC^0)-uniform AC^0 equals FO-uniform AC^0 .)

► **Corollary 26.** $(\text{FO-D-uniform para-AC}^{0\uparrow})\text{-uniform para-AC}^{0\uparrow} = \text{FO-D-uniform para-AC}^{0\uparrow}$.

Proof sketch. If $(L_D(C), \pi_4)$ is in FO-uniform para- $\text{AC}^{0\uparrow}$, then by Theorem 21 it lies in linear-BD-uniform para- $\text{AC}^{0\uparrow}$. Follow the proof of Lemma 24, now using linear-BD-uniform para- $\text{AC}^{0\uparrow}$ -families for the query blocks. ◀

5 Extended uniformity

Thus far we considered direct uniformity notions, where the connection language only contains information on directly related gates. Extended uniformity notions, where the connection language also describes paths between gates, are of interest because logtime-E-uniform circuit classes such as logtime-E-uniform AC^0 and NC^i are equal to natural alternating Turing machine classes [16]. It is unknown whether logtime-D-uniformity and logtime-E-uniformity are equivalent in general, but it has been shown that logtime-D-uniform AC^0 is equal to logtime-E-uniform AC^0 [16, Theorem 4.31]. We will show that this also holds for para- AC^0 and, more interestingly, for para- $\text{AC}^{0\uparrow}$.

► **Definition 27.** *Let C be a circuit. A **path** from gate G to gate G' is a list of steps $p = \langle p_1, p_2, \dots, p_m \rangle$ such that there exist gates G_0, \dots, G_m, G_{m+1} in C where for each i , G_{i+1} feeds into the p_{i+1} th input wire of G_i , with $G_0 = G$ and $G_{m+1} = G'$.*

In the extended connection language, the p in $\langle G, a, p, z, z' \rangle$ are paths from G to a [16].

► **Definition 28.** *Let C be a parameterized circuit family. The **extended connection language** $L_E(C)$ consists of all strings of the form $\langle G, a, p, z, z' \rangle$ where, writing n for $|z|$ and k for $|z'|$:*

1. G is a gate in $C_{n,k}$;
2. if $p = \epsilon$ then $a < 3$ indicates the type of G (one of AND, OR, NOT);
3. otherwise, p is a path from G to a .

In [16, p. 123], Vollmer defines logtime-E-uniformity for non-parameterized polynomial-size constant-depth circuit families C as $L_E(C)$ being in $\text{DTIME}^R(\log n)$. We adapt this to $O(d(k))$ -depth parameterized circuit families as follows.

► **Definition 29.** A parameterized circuit family of size $O(f(k)n^c)$ and depth $O(f(k))$ is **logtime-E-uniform** if $(L_E(C), \pi_4)$ is $\text{DTIME}^R(\log n + g(k))$ for a computable g .

For $\text{para-AC}^{0\uparrow}$, this definition is quite strict: there are logtime-D-uniform circuit families of size $O(f(k)n^c)$ and depth $d(k)$ that contain valid paths p of $d(k)$ steps, where every step has size $\Omega(\log n)$. The encoding of such paths p has length $\Omega(d(k) \log n)$. No $\text{DTIME}^R(\log n + g(k))$ machine in Definition 28 has time to read the complete path p . Nevertheless, these circuit families still have logtime-E-uniform representatives for $\text{para-AC}^{0\uparrow}$.

► **Lemma 30.** Let A be a parameterized circuit family of size $O(f(k)n^c)$ and depth bounded by $d(k)$, with f, d computable. If A is linear-BD-uniform, there is an equivalent logtime-E-uniform circuit family C of size $O(f'(k)n^{c'})$ and depth $O(d(k))$, with f' computable.

Proof sketch. As in the proofs of Lemmas 24 and 25, C will be made up of $d(k)$ layers of simgates. The main idea is that only steps between layers are difficult, and that in order to decide to which simgate a path leads, we only need to read the last inter-layer step. We achieve this by making the number of simgates per layer exactly $2^{L(n,k)} - 1$ for some appropriate $L(n, k)$. Then, if C were to consist only of these simgates, and the simgates were actual gates instead of subcircuits, it could be checked whether a path p moves from simgate $\langle m, q \rangle$ to $\langle m', q' \rangle$ by making sure that

1. each step in p has length at most $L(n, k)$,
2. $d(k) \geq m \geq m' \geq 1$ and p contains $m - m'$ steps, and
3. the last step in p is q' .

So, only the final step in p has to be read. For the others it suffices to read their lengths. From this it can be shown that the whole procedure can be performed in $O(h(k) + \log n)$ time for some computable h . The full version contains a full proof in Appendix B. ◀

Because logtime-E-uniform families of size $O(f(k)n^c)$ and depth $f(k)$ are by definition also logtime-D-uniform and hence (by Theorem 21) equivalent to a linear-BD-uniform family of similar dimensions, we may now conclude the following.

► **Corollary 31.** Logtime-E-uniform $\text{para-AC}^{0\uparrow}$ equals logtime-D-uniform $\text{para-AC}^{0\uparrow}$, and logtime-E-uniform para-AC^0 equals logtime-D-uniform para-AC^0 .

We can also define FO-E-uniformity as $(L_E(C), \pi_4)$ being para-FO. By the same proof as Lemma 20, it can then be shown that logtime-E-uniformity implies FO-E-uniformity for parameterized circuit families of size $O(f(k)n^c)$, and thus (because FO-E-uniformity implies FO-D-uniformity, and by then applying Theorem 21) FO-E-uniform $\text{para-AC}^{0\uparrow}$ is equivalent with logtime-D-uniform $\text{para-AC}^{0\uparrow}$. The same also holds for para-AC^0 .

6 Relation to descriptive complexity

In this section we discuss a descriptive classification of logtime-uniform $\text{para-AC}^{0\uparrow}$ mirroring the equivalence of FO and logtime-uniform AC^0 in Theorem 11.

For non-parameterized circuits, Barrington and Immerman [10] prove that for sufficiently constructible polynomially bounded functions t , logtime-D-uniform and FO-D-uniform $\text{AC}[t(n)]$ are equal to the class $\text{FO}[t(n)]$ of languages decided by iterated first order sentences.

A similar observation can be made in the parameterized setting. Define $\text{para-AC}[f(k)]$ in terms of parameterized circuit families of size $O(f(k)n^c)$ and depth $O(f(k))$, so that $\text{para-AC}^{0\uparrow}$ is the union of $\text{para-AC}[f(k)]$ over the computable functions f . Based on the definition of $\text{FO}[t(n)]$ in [9, Definition 4.24], we define $\text{para-FO}[f(k)]$ as follows.

Write $(\forall x.\phi)\psi$ for $(\forall x)(\phi(x) \rightarrow \psi)$ and $(\exists x.\phi)\psi$ for $(\exists x)(\phi(x) \wedge \psi)$. A **quantifier block** is a partial formula of the form $(Q_0x_0.M_0)(Q_1x_1.M_1)\dots(Q_mx_m.M_m)$, where the Q_i are quantifiers, the x_i are (not necessarily distinct) variable letters, and the M_i are quantifier-free formulas in the language of FO.

► **Definition 32.** A parameterized problem (Q, κ) is in $\text{para-FO}[f(k)]$ if there is a computable g , a quantifier block M , a quantifier-free formula ψ , and a tuple of constants c such that

$$y \models M^{f(\kappa(x))}\psi(c) \iff y \in \{\langle x, g(\kappa(x)) \rangle : x \in Q\}$$

where $M^{f(\kappa(x))}\psi(c)$ stands for the sentence obtained by concatenating $f(\kappa(x))$ copies of M with ψ , and then substituting c_i for free occurrences of variables x_i .

Intuitively, a parameterized problem (Q, κ) is in $\text{para-FO}[f(k)]$ if it is first-order describable in $|x|, f(\kappa(x))$ and iterations of length $f(\kappa(x))$, that is, if $x \in Q \iff x \models M^{f(\kappa(x))}\psi(c)$ holds. That this corresponds with Definition 32 can be made precise by adding constant symbols for $|x|$ and $f(\kappa(x))$ to the language, and extending the domain of x from $|x|$ to $\max(|x|, f(\kappa(x)))$.

Following the proof strategies in [10] (see also [9]) it follows that, writing \mathbf{C} for the computable functions $\mathbb{N} \rightarrow \mathbb{N}$:

$$\text{FO-D-uniform para-AC}^{0\uparrow} = \bigcup_{f \in \mathbf{C}} \text{FO-uniform para-AC}[f(k)] = \bigcup_{f \in \mathbf{C}} \text{para-FO}[f(k)],$$

thus linking logtime-D-uniform $\text{para-AC}^{0\uparrow}$ to a descriptive complexity class. Following [10, 9] further leads to an alternative, descriptive complexity-based proof for Theorem 21.

7 Conclusion

We have shown that, for para-AC^0 and $\text{para-AC}^{0\uparrow}$, various uniformity conditions found in ordinary circuit complexity are again equivalent in the sense that the respective induced complexity classes are equal. This can be used to repair uniformity gaps in the literature.

For example, while our result does not directly demonstrate that the circuit family mentioned in [1, Theorem 3.2] is logtime-D-uniform as claimed, it does prove that there is a suitable logtime-D-uniform circuit family equivalent with it. Since the circuits are described in terms of additions, multiplications, and modulo operations of numbers below a polynomial in n and parameter k , it is straightforward to show that the circuit family is FO-D-uniform, and so, by Theorem 21, there is an equivalent logtime-D-uniform family.

We obtain our equivalences via the stricter parameterized linear-uniformity condition, proving a substitution lemma and then explicitly constructing layered linear-uniform families for given FO-uniform families. In a sense this can be seen as a direct, circuit-oriented variant of the approach in [10]. Here they prove the equivalence of (direct, non-parameterized) uniformity conditions for depth- $t(n)$ circuits via the descriptive complexity class $\text{FO}[t(n)]$, constructing layered logtime-uniform circuits deciding $\text{FO}[t(n)]$ -formulas.

Our results show the equivalence between the uniformity conditions not on the circuit family level but only on the complexity class level. This suffices for theoretical applications like [1, Theorem 3.2] mentioned above, but is not fine-grained enough for questions of work efficiency. For example, the proof of Theorem 21 gives for an FO-D-uniform circuit family of size $f(k)n^c$ a logtime-D-uniform circuit family of size greater than $f(k)n^{3c+1}$. This gap limits the study of open problems in fine-grained parallel complexity. It would therefore be interesting to study the inherent cost of the conversion, and to also consider which uniformity condition is the most natural one from a (parameterized) parallel complexity perspective.

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