


# Smaller Circuits for Bit Addition

**Mikhail Goncharov**

Neapolis University Pafos, Cyprus  
JetBrains Research, Pafos, Cyprus

**Alexander S. Kulikov** ✉ 🏠 

JetBrains Research, Pafos, Cyprus

**Georgie Levtsov**

Neapolis University Pafos, Cyprus  
JetBrains Research, Pafos, Cyprus

---

## Abstract

Bit addition arises virtually everywhere in digital circuits: arithmetic operations, increment/decrement operators, computing addresses and table indices, and so on. Since bit addition is such a basic task in Boolean circuit synthesis, a lot of research has been done on constructing efficient circuits for various special cases of it. A vast majority of these results are devoted to optimizing the circuit *depth* (also known as delay).

In this paper, we investigate the circuit *size* (also known as area) over the full binary basis of bit addition. Most of the known circuits are built from Half Adders and Full Adders as suggested by Dadda in 1965 for designing multiplier circuits. Applying these ideas to the bit addition function, one gets a  $5n - 3m$  upper bound on its circuit size, where  $n$  is the number of input bits and  $m$  is the number of output bits. We prove an upper bound  $4.5n - 2m$ . In the regimes where  $m$  is small compared to  $n$  (for example, for computing the sum of  $n$  bits or multiplying two  $n$ -bit integers), this leads to 10% improvement. We also show that it is provably impossible to improve the two upper bounds above to  $5n - 3.01m$  or  $4.5n - 2.51m$ . We achieve this by establishing that the circuit size of the increment function (a special case of the bit addition function with  $m = n + 1$ ) is equal to  $2n$ .

We complement our theoretical result by an open-source implementation of generators producing circuits for bit addition and multiplication. The generators allow one to produce the corresponding circuits in two lines of code and to compare them to existing designs.

**2012 ACM Subject Classification** Theory of computation → Logic and verification; Theory of computation → Complexity theory and logic; Theory of computation → Circuit complexity

**Keywords and phrases** bit addition, summation, multiplier, multiplication, Boolean, circuit, synthesis, combinational, digital

**Digital Object Identifier** 10.4230/LIPIcs.STACS.2026.46

**Supplementary Material** *Software (Source Code)*: <https://github.com/spbsat/cirbo>  
archived at `swh:1:dir:bb1d9d50044cfe5a05b7c8dad7404b306c90cd1`

**Acknowledgements** We thank the anonymous reviewers for many helpful comments.

## 1 Overview

Bit addition arises virtually everywhere in digital circuits: arithmetic operations, increment/decrement operators, computing addresses and table indices, and so on. Three specific scenarios where it is used frequently are listed below.

- Adding two  $n$ -bit numbers.
- Computing a symmetric Boolean function (such as majority or sorting). A natural way of doing this is to first compute the binary representation of the sum of  $n$  input bits (that is, to compress  $n$  bits into about  $\log_2 n$  bits) and then to compute the function at hand out of the computed binary representation.



© Mikhail Goncharov, Alexander S. Kulikov, and Georgie Levtsov;  
licensed under Creative Commons License CC-BY 4.0

43rd International Symposium on Theoretical Aspects of Computer Science (STACS 2026).

Editors: Meena Mahajan, Florin Manea, Annabelle McIver, and Nguyễn Kim Thăng  
Article No. 46; pp. 46:1–46:15



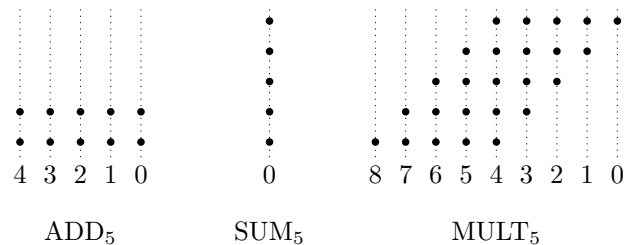
Leibniz International Proceedings in Informatics

Schloss Dagstuhl – Leibniz-Zentrum für Informatik, Dagstuhl Publishing, Germany



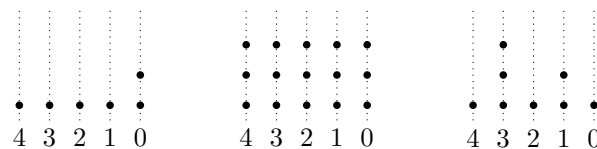
## 46:2 Smaller Circuits for Bit Addition

- To multiply two  $n$ -bit numbers, one may first compute all partial products (that is, products of the bits of the two input numbers) and then sum up the resulting bits. In terms of the dot-notation introduced by Dadda [4], the three scenarios discussed above are visualized as shown in Figure 1. In this notation, one places bits of the same significance on the same vertical layer.



■ **Figure 1** Dot diagrams for three Boolean functions:  $\text{ADD}_5$  adds two five-bit numbers,  $\text{SUM}_5$  adds five bits, and  $\text{MULT}_5$  adds five (appropriately shifted) five-bit numbers.

There are many other cases where one needs to add bits. Say, one may want to add a single bit to an  $n$ -bit number (the increment operation is a special case), or to add three  $n$ -bit numbers, or to add a few bits of varying significance, see Figure 2.



■ **Figure 2** More scenarios of adding bits of varying significance.

A function capturing all such scenarios is known as *bit adder*

$$\text{BA}_n^{s_1, \dots, s_n} : \{0, 1\}^n \rightarrow \{0, 1\}^m.$$

It is parameterized by the *significance vector*  $s = (s_1, \dots, s_n) \in \mathbb{Z}_{\geq 0}^n$ , takes  $n$  input bits  $(x_1, \dots, x_n) \in \{0, 1\}^n$ , and outputs the binary representation of

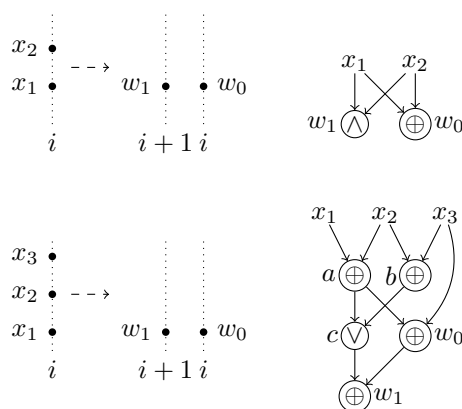
$$\sum_{i=1}^n 2^{s_i} x_i.$$

This way,  $\text{SUM}_n = \text{BA}_n^{0, 0, \dots, 0}$  and  $\text{ADD}_n = \text{BA}_{2n}^{0, 0, 1, 1, \dots, n-1, n-1}$ .

Since bit addition is such a basic task in Boolean circuit synthesis, a lot of research has been done on constructing efficient circuits for various special cases of it, see, for example, [9, 8, 12, 2]. A vast majority of these results is devoted to optimizing the circuit *depth* (also known as delay). In this paper, we investigate the circuit *size* (also known as area) of bit addition. Specifically, we study circuits over the full binary basis.

Two basic building blocks for adding bits are known as Half Adder (HA) and Full Adder (FA). They compute the binary representation of the sum of two and three bits, respectively (that is,  $\text{SUM}_2$  and  $\text{SUM}_3$ ). In the full binary basis, they can be implemented in two and five gates, respectively, see Figure 3.

Using Half Adders and Full Adders, one can synthesize a bit adder using the following algorithm that goes back to Napier's *Rabdologiae* (1617), as modernized by Dadda [4].



■ **Figure 3** The Half Adder (top) and Full Adder (bottom): dot diagrams and circuits.

Process the bits layer by layer, in the order of increasing significance. While the current significance layer  $i$  contains at least three bits, take three of them and apply the Full Adder to replace them with a pair of bits of significance  $i$  and  $i + 1$ . If there are two bits left at the current layer  $i$ , apply the Half Adder to them to get a pair of bits of significance  $i$  and  $i + 1$ .

This algorithm ensures that, for any vector  $s \in \mathbb{Z}_{\geq 0}^n$ ,

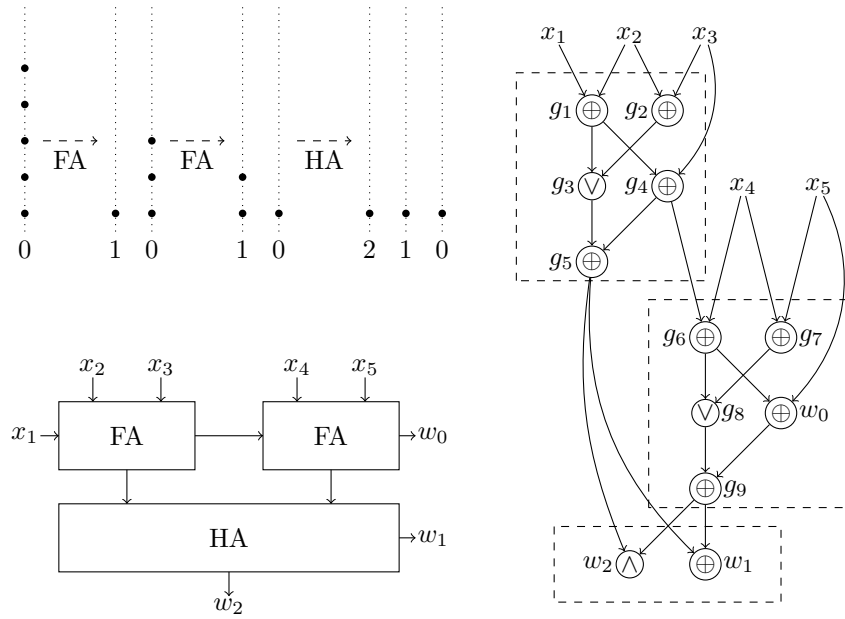
$$\text{size}(\text{BA}_n^s) \leq 5n - 3m.$$

Indeed, each application of the Full Adder reduces the number of bits by one, hence the total cost of all Full Adders is at most  $5(n - m)$ . The Half Adder is applied at most once for each of the significance layers, hence the total cost of all Half Adders is at most  $2m$ . Hence, the total size is at most  $5(n - m) + 2m = 5n - 3m$ . Note that most of the previous works consider specific special cases of bit addition (like summation or multiplication) where  $m$  is a specific function on  $n$ . In such cases, the upper bounds are stated in terms of  $n$  only. The parameter  $m$  arises naturally when one considers the general bit addition function.

By applying this algorithm to partial products of bits of two input  $n$ -bit numbers, one gets the well-known Dadda multiplier circuit [4]. For many vectors  $s$ , the upper bound  $5n - 3m$  is loose: it does not match the size of the actual circuit produced by the algorithm. A straightforward example is  $s = (0, 1, \dots, n - 1)$ : in this case, no gates are needed whereas the upper bound is  $2n$ . It is also worth noting that, in some cases, the resulting circuit is *provably* optimal. For example, for the  $\text{ADD}_n$  function (that computes the sum of two  $n$ -bit integers), the method constructs a circuit out of a single Half Adder and  $(n - 1)$  Full Adders. The resulting circuit is known as *ripple-carry adder* and has size  $5n - 3$ . Red'kin [10] proved that there is no smaller circuit for this function.

At the same time, in many scenarios, not only the bound  $5n - 3m$  is loose, but also the circuit produced by the algorithm is suboptimal. For example, for  $\text{SUM}_5$ , it gives a circuit of size 12 consisting of two Full Adders and one Half Adder, see Figure 4. However,  $\text{SUM}_5$  can be computed by a circuit of size 11 as shown by [7] (see also Figure 7 later in the text). In general, whereas the algorithm produces a circuit of size about  $5n$  for  $\text{SUM}_n$ , this function can be computed by a circuit of size about  $4.5n$  as shown by Demenkov et al. [5].

In this paper, we generalize the construction by Demenkov et al. Namely, we prove an upper bound  $4.5n - 2m$  for the circuit size of bit addition. In the regimes where  $m$  is small compared to  $n$ , this gives a circuit that is about 10% smaller. This applies to the Dadda multiplier. We complement our theoretical result by an open source implementation of generators producing circuits for bit addition and multiplication.



■ **Figure 4** A circuit of size 12 computing  $SUM_5$  composed of two Full Adders and one Half Adder: dot notation (top left), block structure (bottom left), and a circuit (right).

We also show that it is provably impossible to improve the two upper bounds above to  $5n - 3.01m$  or  $4.5n - 2.51m$ . We achieve this by establishing that the circuit size of the increment function (a special case of the bit addition function with  $m = n + 1$ ) is equal to  $2n$ .

## 2 General Setting

In this section, we formally introduce the Boolean functions studied in this paper as well as the main building blocks for computing them.

### 2.1 Boolean Functions

The main Boolean function studied in this paper is *bit adder*

$$BA_n^{s_1, \dots, s_n} : \{0, 1\}^n \rightarrow \{0, 1\}^m.$$

It computes the binary representation of the weighted sum of input bits:

$$\sum_{i=1}^n 2^{s_i} x_i.$$

In most interesting scenarios, all bits of the binary representation of this sum depend on the input and the number of outputs can be expressed as follows:

$$m = \left\lceil \log_2 \left( \sum_{i=1}^n 2^{s_i} + 1 \right) \right\rceil.$$

In such cases,

$$BA(x_1, \dots, x_n) = (y_0, \dots, y_{m-1}) : \sum_{i=1}^n 2^{s_i} x_i = \sum_{i=0}^{m-1} 2^i y_i.$$

However, for some other significance vectors, some of the bits of the binary representation of the sum are identically equal to zero (and thus, do not depend on the input). We exclude such bits from the outputs. Thus, more generally, when we say that

$$\text{BA}(x_1, \dots, x_n) = (y_0, \dots, y_{m-1}),$$

we mean that there exists a vector  $t = (t_0, \dots, t_{m-1}) \in \mathbb{Z}_{\geq 0}$  such that  $t_0 < t_1 < \dots < t_{m-1}$  and

$$\sum_{i=1}^n 2^{s_i} x_i = \sum_{i=0}^{m-1} 2^{t_i} y_i.$$

It is not difficult to see that the vector  $t$  is unique and that  $m \leq n$ .

This way, the goal of bit addition is to “flatten” the distribution of bits, that is, to leave at most one bit at each significance layer. Figure 5 gives an example.



■ **Figure 5** The function  $\text{BA}_7^{0,1,1,5,5,5,6}: \{0, 1\}^7 \rightarrow \{0, 1\}^6$  replaces seven bits of significance  $(0, 1, 1, 5, 5, 5, 6)$  with six bits of significance  $(0, 1, 2, 5, 6, 7)$ .

Many practically important Boolean functions can be computed using bit summation.

- The function  $\text{SUM}_n: \{0, 1\}^n \rightarrow \{0, 1\}^{\lceil \log_2(n+1) \rceil}$  computes the sum of  $n$  bits:

$$\text{SUM}_n(x_1, \dots, x_n) = \text{ADD}_n^{0,0,\dots,0}(x_1, \dots, x_n).$$

- The function  $\text{ADD}_n: \{0, 1\}^{2n} \rightarrow \{0, 1\}^{n+1}$  computes the sum of two  $n$ -bit numbers:

$$\text{ADD}_n(x_0, \dots, x_{n-1}, y_0, \dots, y_{n-1}) = \text{BA}_{2n}^{0,\dots,n-1,0,\dots,n-1}(x_0, \dots, x_{n-1}, y_0, \dots, y_{n-1}).$$

- The function  $\text{MULT}_n: \{0, 1\}^{2n} \rightarrow \{0, 1\}^{2n}$  computes the product of two  $n$ -bit numbers:

$$\text{MULT}_n(x_0, \dots, x_{n-1}, y_0, \dots, y_{n-1}) = \text{BA}_{n^2}^{(i+j)_{0 \leq i, j < n}} \left( (x_i \wedge y_j)_{0 \leq i, j < n} \right).$$

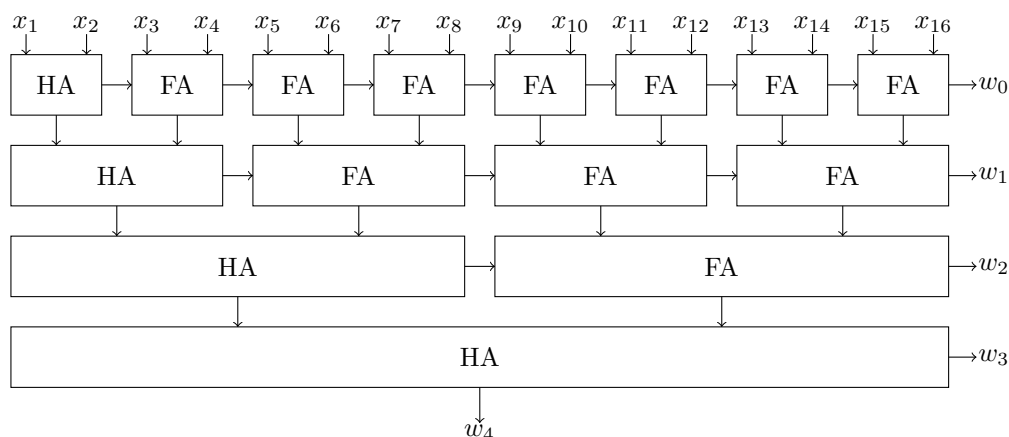
## 2.2 Boolean Circuits

A circuit is a natural way of computing Boolean functions. It is an acyclic directed graph of in-degree 0 and 2 whose  $n + 2$  source nodes are labeled with input variables  $x_1, \dots, x_n$  and constants 0 and 1, whereas all other nodes are labeled with binary Boolean operations. The source nodes are called input gates, all other nodes are called internal gates. Each gate computes a (single-output) Boolean function of  $x_1, \dots, x_n$ . If  $m$  gates of the circuit are marked as outputs, it computes a function of the form  $\{0, 1\}^n \rightarrow \{0, 1\}^m$ . For a circuit  $C$ , its size,  $\text{size}(C)$ , is the number of internal gates of  $C$ , whereas its depth,  $\text{depth}(C)$ , is the maximum length of a path from an input gate of  $C$  to an output gate of  $C$ .

## 2.3 Basic Building Blocks

As discussed before, the Half Adder and Full Adder are basic building blocks for computing bit addition. Figure 6 shows how to synthesize a circuit of size 63 computing  $\text{SUM}_{16}$  out of four Half Adders and eleven Full Adders. It is not difficult to see that a similar block structure can be used for any  $n$  yielding a circuit of size at most  $5n$  for  $\text{SUM}_n$ .

## 46:6 Smaller Circuits for Bit Addition



■ **Figure 6** A circuit computing  $SUM_{16}$  composed out of four Half Adders and eleven Full Adders. Its size is  $4 \cdot 2 + 11 \cdot 5 = 63$ .

It turns out that better circuit designs are possible for  $SUM_n$  as shown by Demenkov et al. [5]. Consider two consecutive Full Adders shown on the top left of Figure 7. The corresponding function DFA (for Double Full Adder) has the following specification:

$$DFA(x_1, x_2, x_3, x_4, x_5) = (b_0, b_1, a_1) : x_1 + x_2 + x_3 + x_4 + x_5 = b_0 + 2(b_1 + a_1).$$

Then, MDFA (for Modified Double Full Adder) has the following specification:

$$MDFA(x_1 \oplus x_2, x_2, x_3, x_4, x_4 \oplus x_5) = (b_0, a_1, a_1 \oplus b_1).$$

That is, for pairs of bits  $(x_1, x_2)$ ,  $(x_4, x_5)$ , and  $(a_1, b_1)$  it uses a slightly different encoding:  $(p, p \oplus q)$  instead of  $(p, q)$ . We call such bits paired and show them in gray boxes in dot diagrams. It allows one to compute MDFA in eight gates (whereas the circuit size of DFA is 10). Moreover, the corresponding circuit of size eight is just a part of an optimal circuit of size 11 computing  $SUM_5$  shown on the right of Figure 7.

We also need a block called MDFA' that can be viewed as a subfunction of MDFA:

$$MDFA'(x_1 \oplus x_2, x_2, x_4, x_4 \oplus x_5) = MDFA(x_1 \oplus x_2, x_2, 0, x_4, x_4 \oplus x_5).$$

It is not difficult to see that one can compute MDFA' using six gates: when one replaces  $x_3$  by zero in the circuit for MDFA, the two gates fed by  $x_3$  can be eliminated. (In the same manner, HA is a subfunction of FA:  $HA(x_1, x_2) = FA(x_1, x_2, 0)$ .)

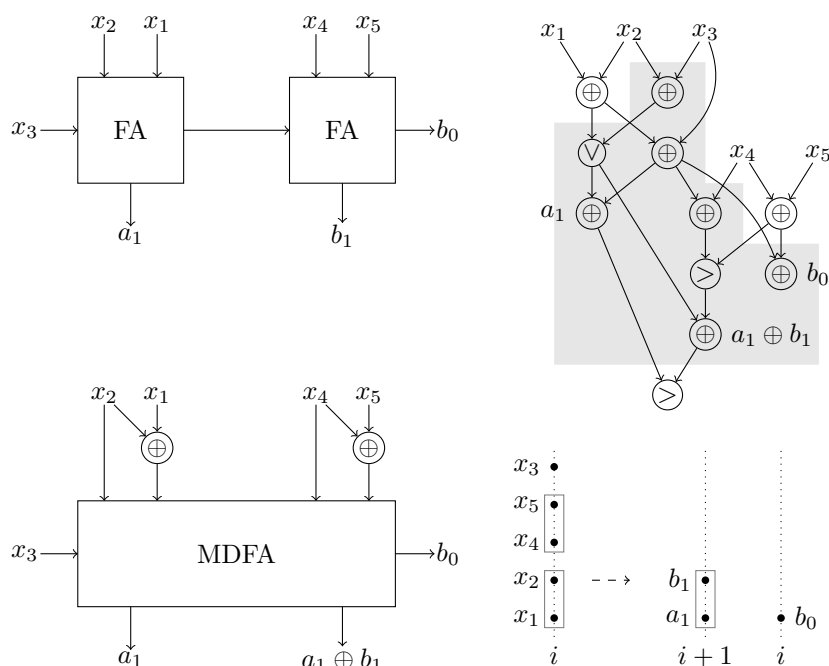
Using MDFA and MDFA' blocks, one can compute  $SUM_n$  roughly as follows:

1. Compute  $x_2 \oplus x_3, x_4 \oplus x_5, \dots, x_{n-1} \oplus x_n$  ( $n/2$  gates).
2. Apply at most  $n/2$  MDFA blocks (no more than  $4n$  gates).
3. The last MDFA block outputs two bits:  $a$  and  $a \oplus b$ . Instead of them, one needs to compute  $a \oplus b$  and  $a \wedge b$ . To achieve this, it suffices to apply  $x > y = (x \wedge \bar{y})$  operation:  $a \wedge b = a > (a \oplus b)$ .

This gives an upper bound  $4.5n$  for  $SUM_n$ , its formal proof can be found in [5]. Figure 8 gives an example of the corresponding design for  $SUM_{16}$ .

### 3 New Upper Bound for Circuit Size of Bit Addition

In this section, we prove a new upper bound  $4.5n - 2m$  for the circuit size of bit addition. For regimes where  $m$  is small compared to  $n$ , this is better than  $5n - 3m$  by about 10%. This applies to  $MULT_n$  and  $SUM_n$ .



■ **Figure 7** Two consecutive Full Adders (top left), the MDFA block (bottom left), an optimal circuit for  $SUM_5$  (top right) whose highlighted part computes MDFA, and a dot diagram for MDFA.

► **Theorem 1.** For any vector  $s \in \mathbb{Z}_{\geq 0}^n$ ,

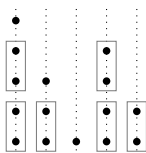
$$\text{size}(BA_n^s) \leq 4.5n - 2m.$$

In the proof, we use the following straightforward observation. Assume that  $s_1 < s_2, s_3, \dots, s_n$ . In this case, the first output is equal to  $x_1$ , the cost of computing this particular bit of the output is zero, allowing one to forget about it. Thus,

$$\text{size}(BA_n^s) = \text{size}(BA_{n-1}^{s'}),$$

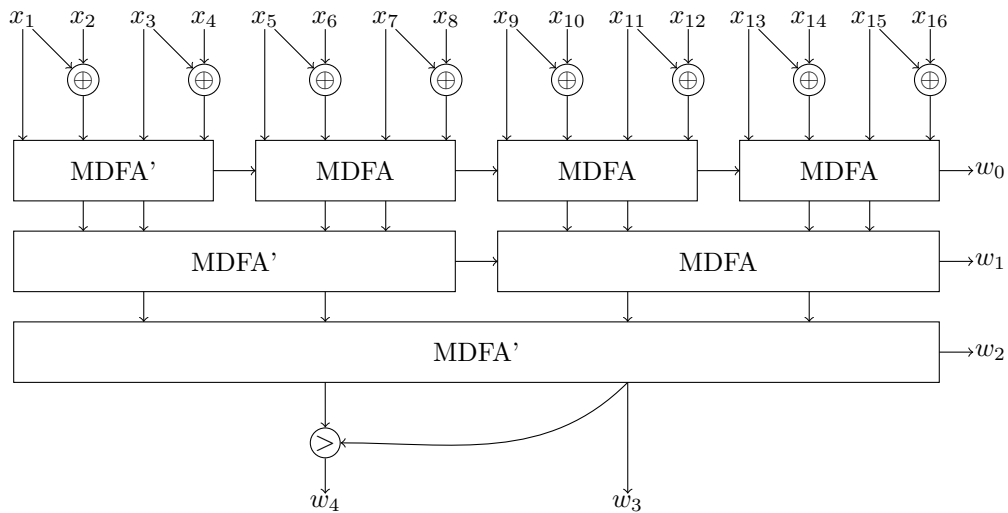
where  $s' = (s_2, \dots, s_n)$ . We call the operation of replacing  $s$  by  $s'$  as *shifting*. Note that shifting reduces both the number of inputs and the number of outputs by one. Figure 9 gives an example.

**Proof.** As the first step, we do the following: at every significance layer, we break all bits, except for possibly one, into pairs and compute the parity for every pair. This takes at most  $n/2$  gates.



Then, it remains to prove that one can compute the sum of  $n$  bits using  $4n - 2m$  gates if every significance layer contains at most one bit without a pair. We prove this by induction on  $n$ . The base case  $n = 1$  is clear: in this case, the circuit size is zero (nothing needs to be summed up) and the upper bound is at least zero since  $m \leq n$ . To prove the induction step, denote by  $l$  the number of minimum elements in the significance vector  $s$  (that is, the number of bits in the rightmost non-empty column in dot-notation).

46:8 Smaller Circuits for Bit Addition



■ **Figure 8** A circuit computing  $SUM_{16}$  composed out of eight  $\oplus$ -gates at the top, three MDFA' blocks, four MDFA blocks, and one final gate. Its size is  $8 + 3 \cdot 6 + 4 \cdot 8 + 1 = 59$ .



■ **Figure 9** Shifting:  $size(BA_3^{2,3,3}) = size(BA_2^{3,3})$ . In turn,  $BA_2^{3,3}$  can be computed by the Half Adder. Thus,  $BA_3^{2,3,3}(x_1, x_2, x_3) = (x_1, x_2 \oplus x_3, x_2 \wedge x_3)$ .

Consider the following seven cases. (In fact, the first three cases are special cases of the last three cases, but we believe that the presentation is cleaner when they are stated as separate cases.) In each of the cases below, we shift and proceed by induction.

1.  $l = 1$ . In this case, we just shift. By the induction hypothesis, the rest can be computed by a circuit of size at most

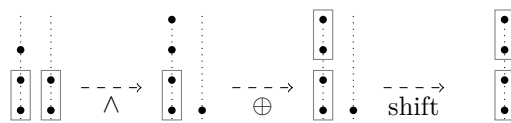
$$4(n - 1) - 2(m - 1) = 4n - 2m - 2 < 4n - 2m.$$

2.  $l = 2$ . Then, the corresponding two bits  $x_1$  and  $x_2$  are paired meaning that their sum  $x_1 \oplus x_2$  is computed already. Then, we compute their carry

$$c = x_1 > (x_1 \oplus x_2) = x_1 \wedge x_2$$

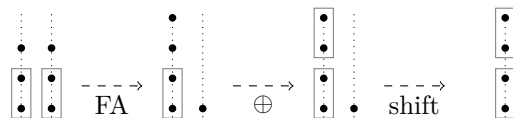
and transfer it to the next layer. If this layer has an unpaired bit  $b$ , we pair  $b$  and  $c$  by computing  $b \oplus c$ . Finally, we shift. By the induction hypothesis, the size of the resulting circuit is at most

$$1 + 1 + 4(n - 1) - 2(m - 1) = 4n - 2m.$$



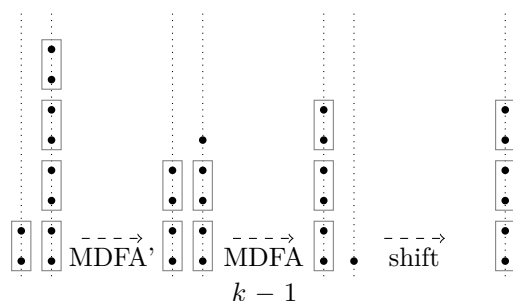
3.  $l = 3$ . For the corresponding three bits  $x_1, x_2, x_3$ , we have  $x_1 \oplus x_2$ ,  $x_2$ , and  $x_3$  (that is,  $x_1$  and  $x_2$  are paired). We apply the Full Adder to the three bits. This costs four gates, as  $x_1 \oplus x_2$  is already computed and  $x_1$  is not needed (recall Figure 3). The sum bit stays on the same layer, whereas the carry bit  $c$  goes to the next layer. Then, we pair  $c$  with an unpaired bit on the next layer if needed and shift. This gives an upper bound

$$4 + 1 + 4(n - 2) - 2(m - 1) < 4n - 2m.$$



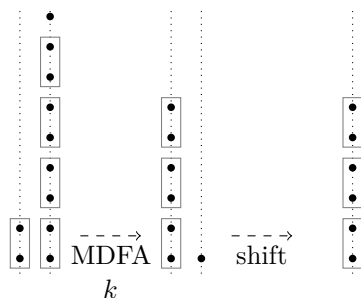
4.  $l = 4k$ . Apply MDFA' to two pairs to produce an unpaired bit. For the remaining  $2k - 2$  pairs, keep applying MDFA, each time reusing the unpaired bit. Then, we shift. The upper bound is

$$6 + 8(k - 1) + 4(n - 2k) - 2(m - 1) = 4n - 2m.$$



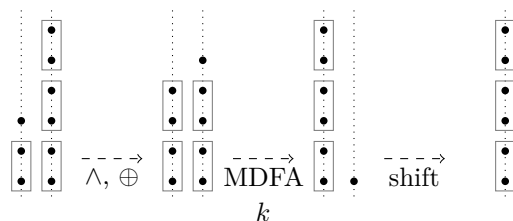
5.  $l = 4k + 1$ . Apply MDFA  $k$  times, then shift. The upper bound is

$$8k + 4(n - 2k - 1) - 2(m - 1) < 4n - 2m.$$

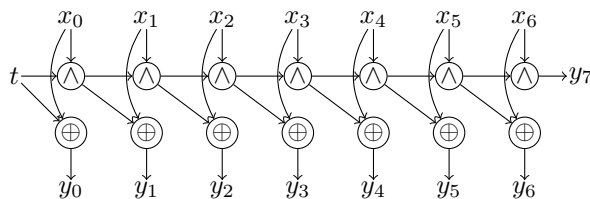


6.  $l = 4k + 2$ . For two bits  $a$  and  $a \oplus b$  from the same pair, compute the most significant bit of their sum using a single binary gate:  $a > (a \oplus b) = a \wedge b$ . This leaves their sum  $(a \oplus b)$  at the current layer and puts the just computed carry bit  $(a \wedge b)$  to the next layer. If needed, compute the parity of an unpaired bit with the just transferred carry bit. Then, apply MDFA  $k$  times and shift. Overall, the upper bound is

$$1 + 1 + 8k + 4(n - 2k - 1) - 2(m - 1) = 4n - 2m.$$



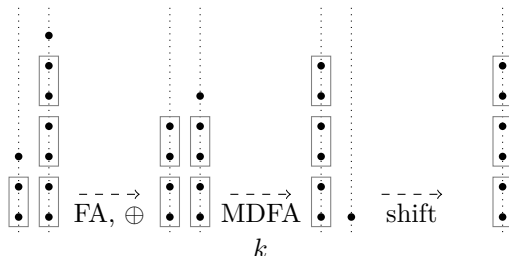
46:10 Smaller Circuits for Bit Addition



■ **Figure 10** One can add a bit  $t$  to a 7-bit integer  $x_0 \cdots x_6$  (to get an 8-bit integer  $y_0 \cdots y_7$ ) using 14 gates. A straightforward generalization of this construction ensures that  $\text{size}(\text{BA}_n^{0,0,1,\dots,n-2}) \leq 2n - 2$ .

7.  $l = 4k + 3$ . Apply the Full Adder to a pair of bits and the unpaired bit. If needed, pair the just transferred carry bit with an unpaired bit from the next layer. Then, apply MDFA  $k$  times and shift. The resulting upper bound is

$$4 + 1 + 8k + 4(n - 2k - 2) - 2(m - 1) < 4n - 2m.$$



4 Lower Bounds and Limitations

The upper bound  $\text{size}(\text{BA}_n^s) \leq 5n - 3m$  holds for any vector  $s$ , but in many scenarios it is loose. For example, for the function

$$\text{ADD}_n = \text{BA}_{2n}^{0,\dots,n-1,0,\dots,n-1},$$

this upper bound turns into  $5 \cdot 2n - 3(n + 1) = 7n - 3$ , whereas  $\text{size}(\text{ADD}_n) = 5n - 3$ . Interestingly, the term  $3m$  in the upper bound  $5n - 3m$  cannot be increased: for any constant  $\alpha > 3$ , there exists a vector  $s$  such that  $\text{size}(\text{BA}_n^s) \geq 5n - \alpha m - O(1)$ . One example of such a vector is  $s = (0, 0, 1, \dots, n - 1)$ . The corresponding function  $\text{BA}_n^s$  adds a bit to an  $n$ -bit number. It is not difficult to see that it can be computed using  $n$  Half Adders (see Figure 10), hence its circuit size is at most  $2n$ . Below, we show that this straightforward circuit is optimal (up to an additive constant). It also shows that it is impossible to improve our upper bound  $4.5n - 2m$  to  $4.5n - \beta m$  for  $\beta > 2.5$ .

► **Theorem 2.**

$$\text{size}(\text{BA}_n^{0,0,1,\dots,n-1}) \geq 2n - O(1).$$

**Proof.** Assume that a bit to be added is equal to one (clearly, this only makes the function easier to compute). In other words, we consider the *increment* function  $\text{INC}_n: \{0, 1\}^n \rightarrow \{0, 1\}^{n+1}$ . Thus,  $\text{INC}_n(x_0, \dots, x_{n-1}) = (y_0, \dots, y_n)$  such that

$$1 + \sum_{i=0}^{n-1} 2^i x_i = \sum_{i=0}^n 2^i y_i.$$

It is not difficult to write down explicit formulas for all output bits of  $\text{INC}_n$ . For example, for  $n = 5$ , they are expressed as follows:

$$\begin{aligned} y_0 &= 1 \oplus x_0 \\ y_1 &= x_0 \oplus x_1 \\ y_2 &= x_0 x_1 \oplus x_2 \\ y_3 &= x_0 x_1 x_2 \oplus x_3 \\ y_4 &= x_0 x_1 x_2 x_3 \oplus x_4 \\ y_5 &= x_0 x_1 x_2 x_3 x_4 \end{aligned}$$

We prove that  $\text{size}(\text{INC}_n) \geq 2n - 2$  by induction on  $n$ . The base case  $n = 1$  is clear. For the induction step, take an optimal circuit computing  $\text{INC}_n$  and consider its (topologically) first gate  $A(x_i, x_j)$ .

Now, if both the variables  $x_i$  and  $x_j$  had out-degree one, the whole circuit would depend on  $x_i$  and  $x_j$  through the gate  $A$  only. This would mean that there are two different pairs of constant  $(a_i, a_j), (b_i, b_j) \in \{0, 1\}^2$  such that  $A(a_i, a_j) = A(b_i, b_j)$ . This, in turn, would mean that the circuit does not distinguish between assignments

$$x_i \leftarrow a_i, x_j \leftarrow a_j \text{ and } x_i \leftarrow b_i, x_j \leftarrow b_j.$$

But such a circuit cannot compute the function  $\text{INC}_n$  as  $\text{INC}_n$  clearly distinguishes all four different assignments to  $x_i$  and  $x_j$ .

Thus, assume that, say,  $x_i$  feeds at least two gates. Then, assign  $x_i \leftarrow 1$  and simplify the circuit. During the simplification, the gates fed by  $x_i$  are eliminated. (If a gate fed by  $x_i$  becomes a negation of its other input under an assignment  $x_i \leftarrow 1$ , this negation is incorporated into the Boolean binary operations computed by the successors of this gate.) Also, the resulting circuit computes  $\text{INC}_{n-1}$ . To see this, it is instructive to get back to the previous toy example where  $n = 5$ . Say, we assign  $x_2 \leftarrow 1$ . Then, the outputs are simplified as follows:

$$\begin{aligned} y_0 &= 1 \oplus x_0 \\ y_1 &= x_0 \oplus x_1 \\ y_2 &= x_0 x_1 \oplus 1 \\ y_3 &= x_0 x_1 \oplus x_3 \\ y_4 &= x_0 x_1 x_3 \oplus x_4 \\ y_5 &= x_0 x_1 x_3 x_4 \end{aligned}$$

By ignoring the output  $y_2$ , one gets a function computing  $\text{INC}_4$ :

$$(y_0, y_1, y_3, y_4, y_5) = \text{INC}_4(x_0, x_1, x_3, x_4).$$

By the induction hypothesis, the simplified circuit contains at least  $2(n - 1) - 2 = 2n - 4$  gates. Thus, the original circuit has size at least  $2 + 2n - 4 = 2n - 2$ . ◀

## 5 Implementation and Experimental Evaluation

We implemented efficient generators of our new circuits in the `Cirbo` open-source framework [1]. To generate a circuit computing  $\text{BA}_n^s$ , one passes the vector  $s$ . Listing 1 shows how to use the generator to produce an efficient circuit computing  $\text{SUM}_{31}$  in a single line of code. When the circuit is generated, one can use a wide range of `Cirbo` methods to analyze and manipulate the circuit.

■ **Listing 1** Generating an efficient circuit for  $SUM_{31}$  (that computes the binary representation of the sum of 31 bits). The code also prints the size of the resulting circuit and draws it.

```
from cirbo.synthesis.generation.arithmetics.summation
    import generate_add_weighted_bits_efficient

ckt = generate_add_weighted_bits_efficient([0] * 31)
print(ckt.gates_number())
ckt.view_graph()
```

## 5.1 Adding Bits and Integers

Table 1 compares the size of circuits for  $SUM_n$  composed out of Full Adders with circuits composed out of MDFA blocks (that can be generated using our new method), for various  $n$ . As the table reveals, for large values of  $n$ , the latter circuits are about 10% smaller than the former ones. Also, Listing 2 ensures that for the addition of two  $n$ -bit integers the generator produces circuits of size  $5n - 3$ . Recall that  $ADD_n = BA_{2n}^{0, \dots, n-1, 0, \dots, n-1}$  and that  $5n - 3$  is provably optimal circuit size for this function as shown by Red'kin [10].

■ **Table 1** Comparing the size of circuits for  $SUM_n$  composed out of Full Adders with circuits composed out of MDFA. The bottom row shows the improvement in percents.

$n$	7	31	127	511	2047	8191	32767	131071
FA	20	130	600	2510	10180	40890	163760	655270
MDFA	19	119	543	2263	9167	36807	147391	589751
Improvement	5.0%	8.5%	9.5%	9.8%	10.0%	10.0%	10.0%	10.0%

■ **Listing 2** Ensuring that the generator produces circuits of size  $5n - 3$  for  $ADD_n$ .

```
from cirbo.synthesis.generation.arithmetics.summation
    import generate_add_weighted_bits_efficient as generate

for n in range(2, 100):
    ckt = generate(list(range(n)) + list(range(n)))
    assert ckt.gates_number() == 5 * n - 3
```

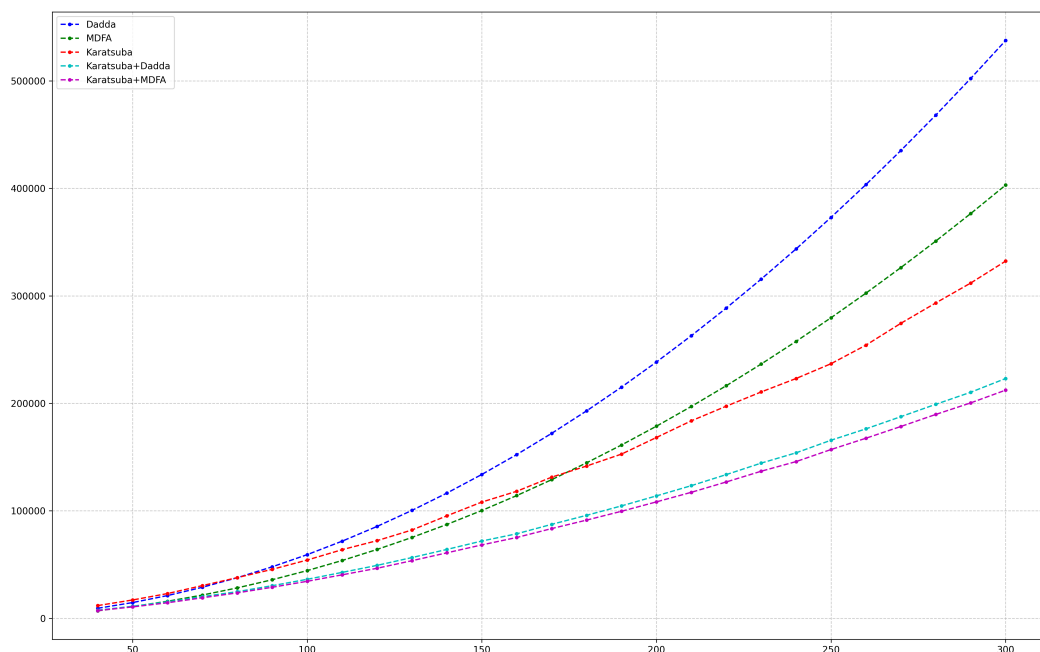
## 5.2 Multiplying Integers

Dadda's multiplier is one of the first circuit designs for multiplying  $n$ -bits integers. Basically, it adds the partial products (conjunctions of the bits of the two input numbers) using Full Adders and Half Adders. Its size is about  $n^2 + 5n^2 = 6n^2$ . Our method of summing up bits allows to reduce the size to roughly  $5.5n^2$ . An asymptotically faster method of multiplying  $n$ -bit integers was discovered by Karatsuba [6]. It is based on the divide-and-conquer approach: to multiply two  $n$ -bit integers, it makes three recursive calls to multiply two  $n/2$ -bit integers and then combines them using summation and subtraction only. This way, the running time  $T(n)$  of the algorithm satisfies a recurrence  $T(n) \leq 3T(n/2) + O(n)$ , hence  $T(n) = O(n^{\log_2 3})$ . As with many other algorithms based on divide-and-conquer,

when  $n$  becomes small, it is beneficial to multiply the given numbers directly (rather than recursively). We implemented generators based on Karatsuba algorithm that use Dadda multipliers and MDFA-based bit addition when  $n$  is smaller than 20. Table 2 and Figure 11 compare the size of the corresponding five circuit designs for  $40 \leq n \leq 300$ . More accurate estimates on the circuits size of multipliers are given by Sergeev [11].

■ **Table 2** Comparing the size of circuits for  $\text{MULT}_n$ . The first multiplier, Dadda, computes the sum of the partial products using Full Adders and Half Adders. The second one, MDFA, sums up the partial products using MDFA blocks. The third one, Karatsuba, makes three recursive calls and recurses all the way down to 4-bit numbers. The fourth and fifth multipliers use Karatsuba algorithm, but switch to Dadda or MDFA multipliers when  $n$  becomes smaller than 20. The last row shows size improvement of the fifth multiplier over the fourth one.

$n$	40	80	120	160	200	240	280
Dadda	9280	37760	85440	152320	238400	343680	468160
MDFA	8539	34679	78419	139759	218699	315239	429379
Karatsuba	11789	37836	72209	118152	168200	223093	293405
Karatsuba, Dadda	7522	24770	49200	78598	113870	153948	199102
Karatsuba, MDFA	7155	23642	46504	75168	108284	145787	189657
Improvement	4.9%	4.6%	5.5%	4.4%	4.9%	5.3%	4.7%



■ **Figure 11** Comparing the size of five circuit designs for  $\text{MULT}_n$ , for  $40 \leq n \leq 300$ .

### 5.3 Logarithmic Depth

The depth of most of the circuits described above is linear, that is,  $\Theta(n)$ . With an additional care, one can make the depth logarithmic ( $\Theta(\log n)$ ) by increasing the size slightly. To achieve this, one processes the layers in parallel rather than consecutively. Namely, let  $h$  be the maximum height of a significance layer (that is, every layer contains at most  $h$  bits). While

$h > 3$ , apply in parallel as many FA's as possible to every layer. After one such step, the maximum height becomes at most  $2h/3$  (to simplify the exposition, we ignore constant additive terms here): indeed, if there are  $k \leq h$  bits on the current layer, then about  $k/3 \leq h/3$  bits remain after the application of FA's; also, at most  $h/3$  bits are transferred from the next layer. Since the maximum height decreases geometrically, in at most  $O(\log n)$  steps, one reaches the case when  $h \leq 3$ . This takes depth  $O(\log n)$  and size  $O(n)$  (since each FA reduces the total number of bits by one). When  $h \leq 3$ , apply either HA or FA to every layer. This ensures that every layer has at most two bits, that is,  $h \leq 2$  (the size of the resulting circuit is still linear and the depth is still logarithmic). Then, everything boils down to adding two  $k$ -bit numbers (with  $k \leq n$ ). This can be performed using, for example, the Brent–Kung adder [3] that has size  $O(k)$  and depth  $O(\log k)$ . By using MDFA's instead of FA's, one can further reduce the size of the resulting circuits. Table 3 shows the size and the depth of the circuits generated this way for the three previously considered functions: SUM, ADD, and MULT.

■ **Table 3** The size and the depth of circuits computing  $\text{SUM}_n$ ,  $\text{ADD}_n$ , and  $\text{MULT}_n$ .

$n$	10	20	30	40	60	80	160	320	
ADD	15	18	23	24	28	31	32	42	depth
	49	101	153	194	297	383	755	1526	size
SUM	10	14	16	18	20	22	26	30	depth
	64	141	215	298	452	615	1252	2529	size
MULT	29	39	46	51	55	62	70	81	depth
	627	2301	5209	9158	20356	35971	142388	566539	size

## 6 Conclusion and Further Directions

In this paper, we presented smaller circuits for bit addition. In many practically relevant scenarios, the described circuits are about 10% smaller than the known circuits composed out of Half Adders and Full Adders. Also, we implemented generators that allow one to produce the corresponding circuits using a single line of code via the Cirbo open-source package [1].

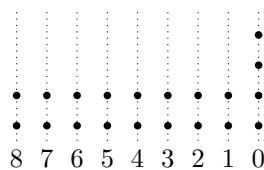
There are three natural open problems related to the circuit size of bit addition.

1. What is the largest  $\alpha$  such that

$$\text{size}(\text{BA}_n^s) \leq 4.5n - \alpha m$$

holds for every vector  $s$ ? In this paper, we proved that  $\alpha \geq 2$ . Theorem 1 shows that  $\alpha \leq 2.5$ . An example of a vector where our upper bound  $4.5n - 2m$  matches the size of the circuit produced by our algorithm is

$$s^* = \left(0, 0, 0, 0, 1, 1, 2, 2, \dots, \frac{n}{2} - 2, \frac{n}{2} - 2\right).$$



In this case, our method first spends  $n/2$  gates to pair the bits and then applies  $n/2$  MDFA' blocks. The size of the resulting circuit is, up to an additive constant,  $n/2 + 6 \cdot n/2 = 3.5n$ . This matches the upper bound  $4.5n - 2m$ . Thus, to improve the bound  $4.5n - 2m$  to  $4.5n - \beta m$ , for  $\beta > 2$ , one needs to find a smaller circuit for this particular vector  $s^*$ . And vice versa, by proving a lower bound  $\text{size}(\text{BA}_n^{s^*}) \geq 3.5n - O(1)$ , one would prove that  $\alpha = 2$ .

2. What is the smallest  $\gamma$  such that

$$\text{size}(\text{BA}_n^s) \leq \gamma n - O(m)$$

holds for every vector  $s$ ? In this paper, we proved that  $\gamma \leq 4.5$ . Improving this seems to be more challenging than just improving  $2m$  to  $2.5m$  as this would most probably require using new building blocks.

3. Finally, note also that the upper bounds  $5n - 3m$  and  $4.5n - 2m$  hold for *all* vectors  $s$ . It would be interesting to improve known upper and lower bounds for *specific* vectors. Perhaps, one of the most interesting such functions is  $\text{SUM}_n$  (here,  $s = (0, 0, \dots, 0)$ ). For it, we know an upper bound  $4.5n$  (originally proved by Demenkov et al. [5]; also follows from our Theorem 1) and a lower bound  $2.5n - O(1)$  due to Stockmeyer [13].

---

## References

- 1 Daniil Averkov, Tatiana Belova, Gregory Emdin, Mikhail Goncharov, Viktoriia Krivogornitsyna, Alexander S. Kulikov, Fedor Kurmazov, Daniil Levtsov, Georgie Levtsov, Vsevolod Vaskin, and Aleksey Vorobiev. Cirbo: A new tool for Boolean circuit analysis and synthesis. In *AAAI*, pages 11105–11112. AAAI Press, 2025. doi:10.1609/AAAI.V39I11.33207.
- 2 K'Andrea C. Bickerstaff, Earl E. Swartzlander Jr., and Michael J. Schulte. Analysis of column compression multipliers. In *IEEE Symposium on Computer Arithmetic*, pages 33–39. IEEE Computer Society, 2001. doi:10.1109/ARITH.2001.930101.
- 3 Richard P. Brent and H. T. Kung. A regular layout for parallel adders. *IEEE Transactions on Computers*, C-31(3):260–264, 1982. doi:10.1109/TC.1982.1675982.
- 4 Luigi Dadda. Some schemes for parallel multipliers. *Alta Frequenza*, 34(5):349–356, 1965.
- 5 Evgeny Demenkov, Arist Kojevnikov, Alexander S. Kulikov, and Grigory Yaroslavtsev. New upper bounds on the Boolean circuit complexity of symmetric functions. *Inf. Process. Lett.*, 110(7):264–267, 2010. doi:10.1016/J.IPL.2010.01.007.
- 6 Anatoly Karatsuba and Yury Ofman. Multiplication of many-digital numbers by automatic computers. *Proceedings of the USSR Academy of Sciences*, 145:293–294, 1962.
- 7 Alexander S. Kulikov, Danila Pechenev, and Nikita Slezkin. SAT-based circuit local improvement. In *MFCS*, volume 241 of *LIPICs*, pages 67:1–67:15. Schloss Dagstuhl – Leibniz-Zentrum für Informatik, 2022. doi:10.4230/LIPICs.MFCS.2022.67.
- 8 Charles U. Martel, Vojin G. Oklobdzija, R. Ravi, and Paul F. Stelling. Design strategies for optimal multiplier circuits. In *IEEE Symposium on Computer Arithmetic*, pages 42–49. IEEE Computer Society, 1995. doi:10.1109/ARITH.1995.465378.
- 9 Mike Paterson and Uri Zwick. Shallow circuits and concise formulae for multiple addition and multiplication. *Comput. Complex.*, 3:262–291, 1993. doi:10.1007/BF01271371.
- 10 Nikolay Red'kin. Minimal realization of a binary adder. *Problemy kibernetiki*, 38:181–216, 1981. In Russian.
- 11 Igor S. Sergeev. On the circuit complexity of the standard and the Karatsuba methods of multiplying integers. In *Information tools and technologies*, volume 3, pages 180–187, 2016. In Russian. English version is available at <http://arxiv.org/abs/1602.02362>. arXiv:1602.02362.
- 12 Paul F. Stelling, Charles U. Martel, Vojin G. Oklobdzija, and R. Ravi. Optimal circuits for parallel multipliers. *IEEE Trans. Computers*, 47(3):273–285, 1998. doi:10.1109/12.660163.
- 13 Larry J. Stockmeyer. On the combinational complexity of certain symmetric Boolean functions. *Math. Syst. Theory*, 10:323–336, 1977. doi:10.1007/BF01683282.