Machine Learning for Timing Analysis: The Good, the Bad and the Ugly

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Abstract

The microarchitecture of processors is becoming increasingly complex and less documented, making the design of timing models for WCET calculation increasingly complicated, if not impossible. We have recently experimented with the use of machine learning techniques (ML) to predict the WCET of basic blocks [3, 1, 2, 4, 5]. Predicted WCETs can then be integrated into static WCET calculation tools, resulting in a hybrid WCET calculation.

In this keynote, we present our experience using ML for WCET calculation, across a range of architectures, from very simple ones (MSP430, Cortex M4) to more complex architectures. Rather than presenting only what worked, we also discuss in this keynote the bad, and even very bad, surprises encountered during the process, and how we overcame (most of) them.

References

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