The Sunflower Tool Suite — Hardware and Software Research Platforms for Energy-Constrained and Failure-Prone Systems

Phillip Stanley-Marbell

Technische Universiteit Eindhoven,
Den Dolech 2, Eindhoven 5612 AZ, The Netherlands.

Abstract. Research in any field requires tools that enable modeling system characteristics of interest. Such tools, whether analytic, simulative, or hardware-based, must enable the accurate evaluation of relevant aspects of a system that may influence its perceived utility.

In computing systems research, software tools (notably, simulators) provide low-cost, flexible, and low turn-around time facilities for investigations, but abstract away many hardware details, often resulting in a loss in accuracy of modeling. Hardware implementations provide the ultimate proofs of concept, but require hardware design expertise, are usually expensive and inflexible, and are not always designed to expose all possible system parameters to researchers. They are also rarely the subject of active evolution over time as research platforms in their own right, as software tools are.

The Sunflower tool suite is a suite of hardware platforms and simulation tools, intended to address these concerns. It comprises a full-system (embedded microarchitecture, networking, power, battery, device failure and analog signal modeling) simulator, a miniature energy-scavenging hardware platform, and a handheld computing device (under development). The suite is intended to provide a set of complementary platforms for research in micro- and system-architectures for embedded systems, with emphases on energy-efficiency, fault-tolerance, and ecological impact of deployed hardware.

1 Overview

There exist an abundance of tools for many aspects of computing systems research, from microarchitectural simulators that are the mainstay of computer architecture research [1], to networking simulators [2] and other domain-specific tools. Academic research tools are seldom calibrated against specific hardware platforms during their development and evolution, and retrospective comparisons often yield interesting observations [3,4]. Even when the simulation platforms are indeed calibrated against hardware, there is seldom the opportunity to evolve the hardware platforms in question. This is due both to the expertise required for implementing hardware designs, as well as the cost of fabrication of hardware prototypes. For high-performance computing systems research, the RAMP platform [5] addresses many of these concerns, providing an open platform for research into multiprocessor architectures.

Dagstuhl Seminar Proceedings 07041
Power-aware Computing Systems
http://drops.dagstuhl.de/opus/volltexte/2007/1106

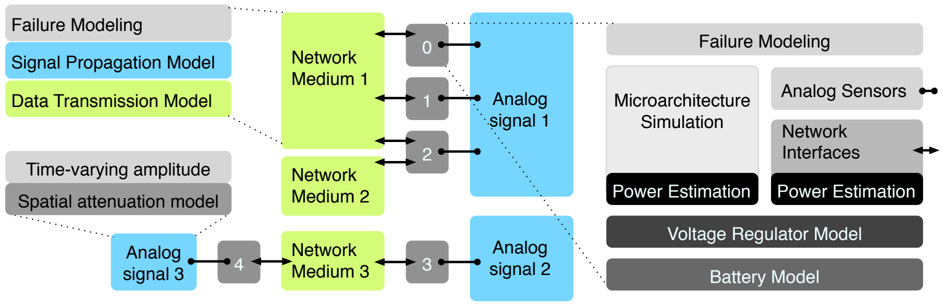

Fig. 1. Illustrative example of the Sunflower full-system simulator's organization.

The goal of the Sunflower tool suite is to provide an actively evolving ecosystem of both hardware prototypes and simulation / analysis tools, for low-power embedded systems, with an emphasis on the investigation of issues relating to energy-efficiency, energy acquisition, fault-tolerance, and impact of hardware deployments on the environment.

On the side of simulation, the Sunflower full-system simulator [6] (Figure 1) enables the evaluation of micro and system-architectures for networked embedded systems, modeling many aspects of both the hardware platforms and the environments within which they execute.

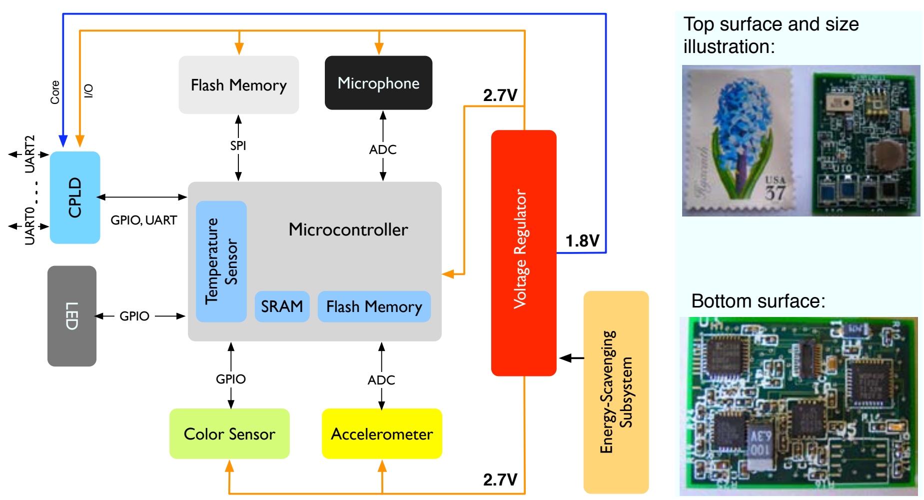

Fig. 2. System architecture of the Sunflower sensor platform (left), and pictures of the current hardware prototype (right).

The Sunflower sensor platform [7] (Figure 2), is one physical realization of components modeled within the Sunflower full-system simulator, enabling the calibration and validation of simulator configurations against real hardware implementations. Additional hardware platforms with complementary hardware capabilities (e.g., wireless communication interfaces and graphical displays) are planned, and it is intended to employ these platforms as a framework for the implementation of ideas by a community of researchers who may not necessarily have interests or expertise in hardware design, but might require specific hardware facilities to enable the investigation of novel software algorithms. For example, researchers investigating dynamic power adaptation algorithms may benefit symbiotically from hardware implementations within the Sunflower framework, of ideas from research groups investigating, e.g., hardware facilities for dynamic voltage and frequency setting, high-efficiency voltage regulators, battery state-of-charge estimators or high-efficiency maximum power point trackers (MPPT).

Providing a means for a research community to submit requests for design extensions, and providing regular (e.g., bi-yearly) updates of the hardware designs which incorporate these research proposals, will hopefully facilitate the validation, in hardware, of research ideas that were previously only investigated in simulation. For such frequent iterations of hardware designs, it will be most practical to make the CAD design files for these design iterations publicly available at no cost, and to ease the fabrication and assembly of small quantities of board-level designs, through appropriate documentation and automated processes.

The tool suite is available online, at `http://www.sflr.org`.

References

1. Burger, D., Austin, T., Bennett, S.: Evaluating Future Microprocessors: The SimpleScalar ToolSet. Technical Report CS-TR-1308, Computer Sciences Department, University of Wisconsin-Madison (1996)
2. `http://www.isi.edu/nsnam/ns/`: ns-2 Network Simulator. (accessed April 2007)
3. Gibson, J., Kunz, R., Ofelt, D., Horowitz, M., Hennessy, J., Heinrich, M.: Flash vs. (simulated) flash: closing the simulation loop. SIGPLAN Not. **35** (2000) 49–58
4. Langendoen, K.: Apples, oranges, and testbeds. In: 2006 IEEE International Conference on Mobile Adhoc and Sensor Systems (MASS). (2006) 387 – 396
5. Arvind, Asanovic, K., Chiou, D., Hoe, J.C., Kozyrakis, C., Lu, S.L., Oskin, M., Patterson, D., Rabaey, J., Wawrzynek, J.: Ramp: Research accelerator for multiple processors — a community vision for a shared experimental parallel hw/sw platform. Technical Report UCB/CSD-05-1412, EECS Department, University of California, Berkeley (2005)
6. Stanley-Marbell, P., Marculescu, D.: Sunflower: Full-System, Embedded Microarchitecture Evaluation. 2nd European conference on High Performance Embedded Architectures and Computers (HiPEAC 2007) / Lecture Notes on Computer Science **4367** (2007) 168–182
7. Stanley-Marbell, P., Marculescu, D.: An 0.9 x 1.2", low power, energy-harvesting system with custom multi-channel communication interface. In: DATE '07: Design Automation and Test in Europe. (2007) 15 – 20